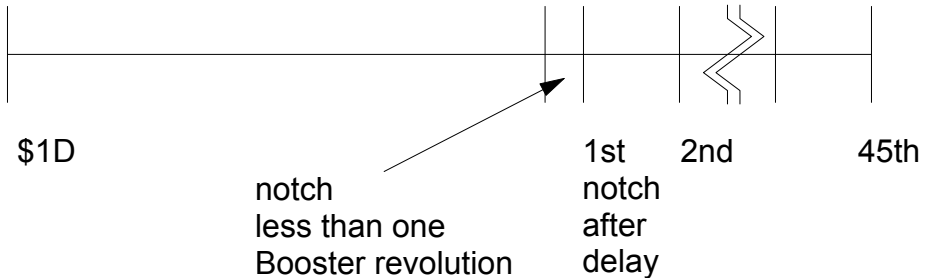


\$1D is synced to Imin in Booster ramp. The Booster is a big, 15 Hz, resonant circuit.

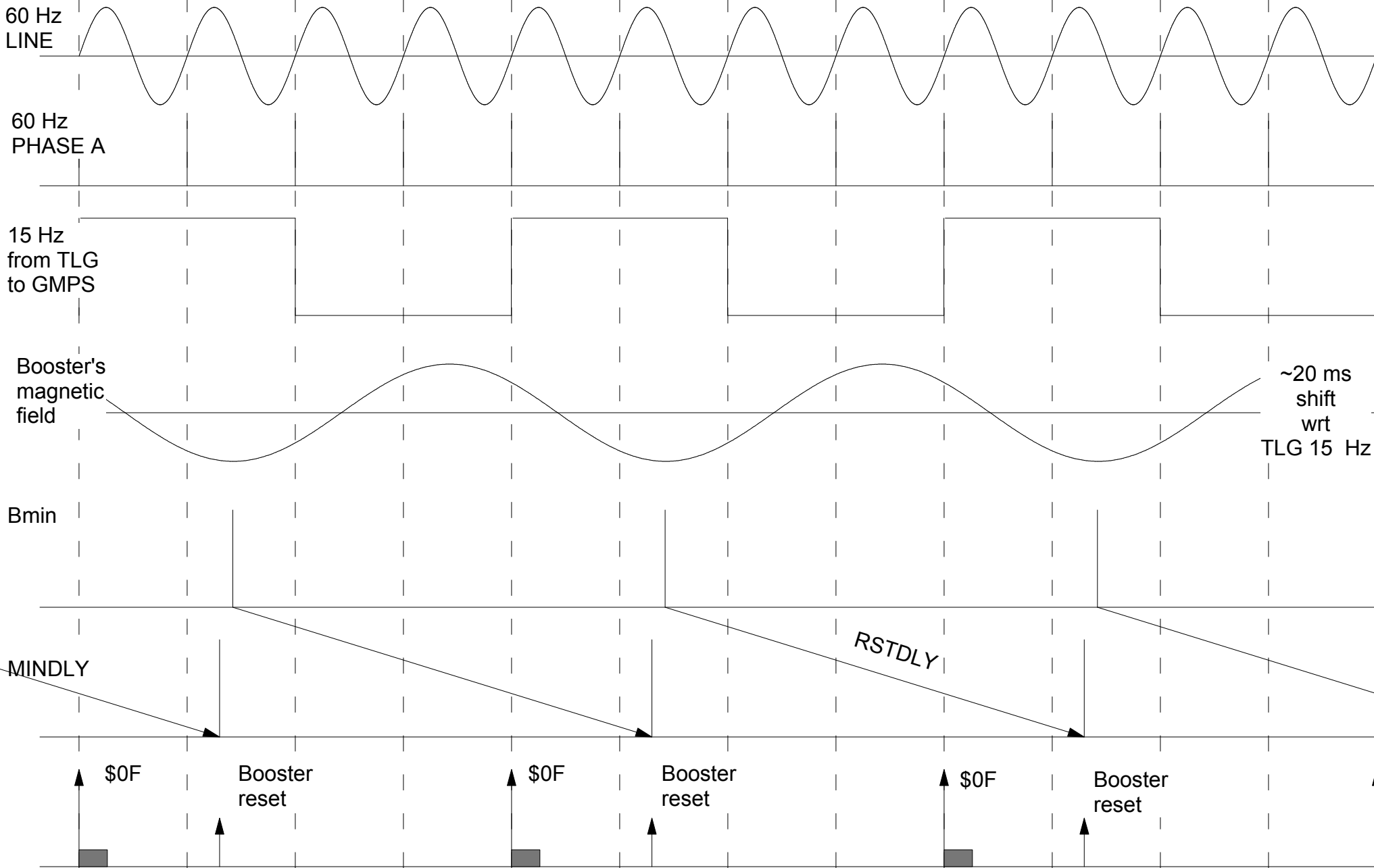
Imin from previous cycle is used to sync current cycle. At Imin, signal goes to Mac room where a delay (G:RSTDLY) is added and TLG creates next Booster Reset.

$228670 \times 1/65 \text{ MHz}$
~35.181 ms

~0.070 ms



Tom Kobilarcik
11/02/2015
information provided by
Kiyomi Seiya
Bill Pellico
Kent Triplett



~20 ms shift wrt TLG 15 Hz

RSTDLY

After \$0F, TLG does an IP bus load. This loads all events into the IP's that will be read out next cycle

The Booster event that was previously loaded (just 18 ms earlier) is now broadcast by the TLG

The non-Booster events that were loaded after previous \$0F are now broadcast by TLG

To make the bminly pulses:
 At Bmin, a delay begins via RSTDLY of 64.654 ms.
 When the delay times out, a bminly pulse is produced ~2ms prior to Bmin of the following Bmin

Info from Kent Triplett