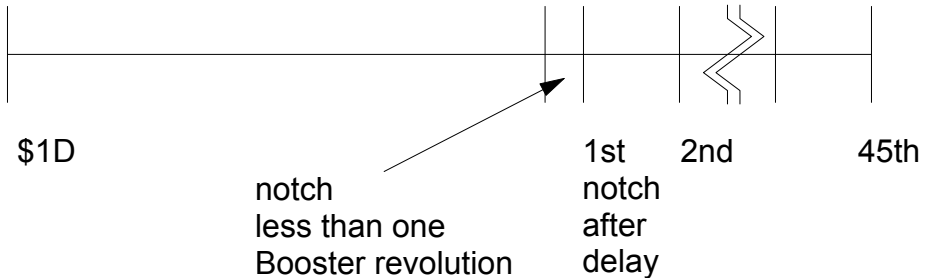


\$1D is synced to Imin in Booster ramp. The Booster is a big, 15 Hz, resonant circuit.

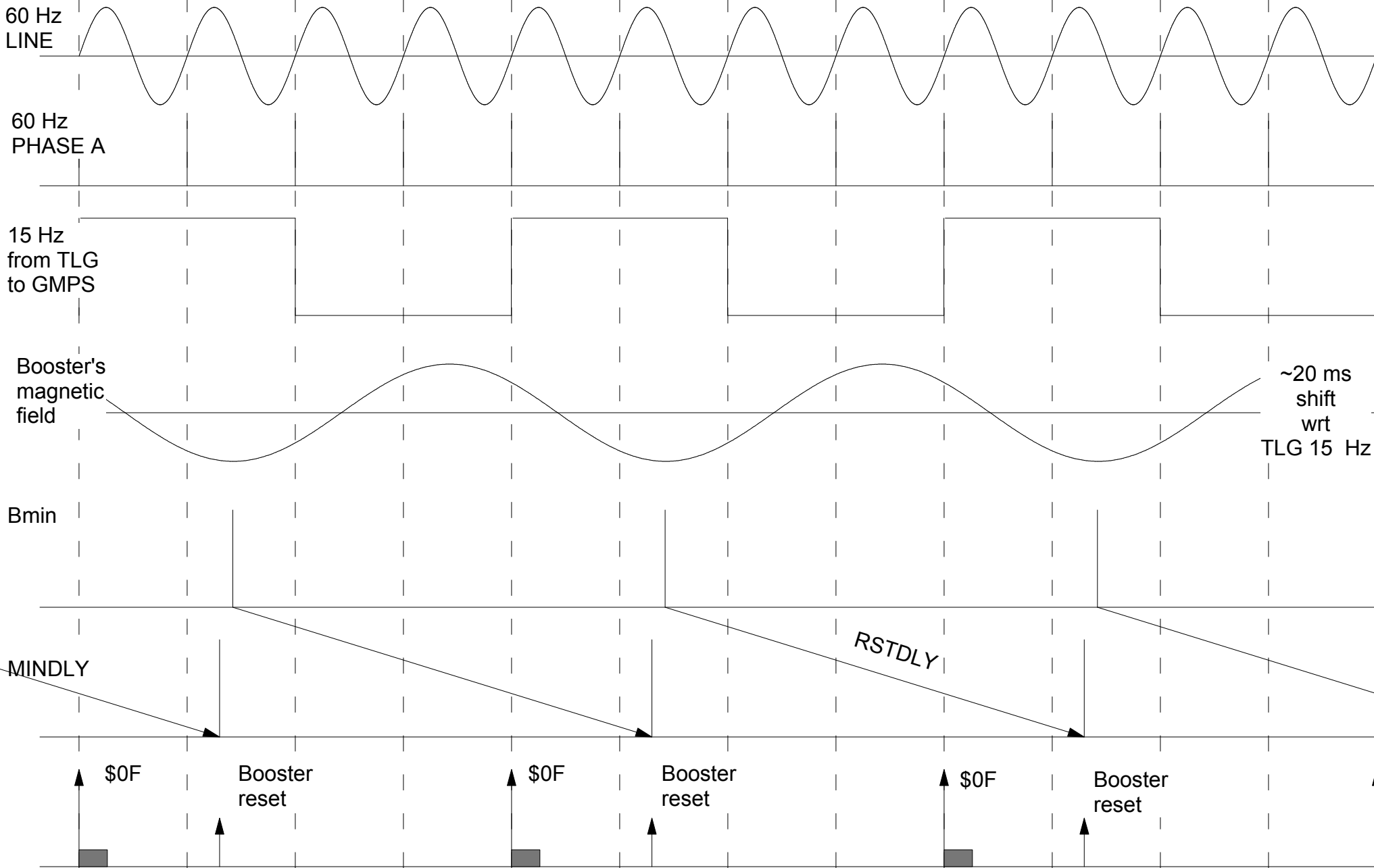
Imin from previous cycle is used to sync current cycle. At Imin, signal goes to Mac room where a delay (G:RSTDLY) is added and TLG creates next Booster Reset.

$228670 \times 1/65 \text{ MHz}$   
 $\sim 35.181 \text{ ms}$        $\sim 0.070 \text{ ms}$



100 ns jitter possible to get bumped by 1.2 us

Tom Kobilarcik  
 10/08/2015  
 information provided by  
 Kiyomi Seiya  
 Bill Pellico  
 Kent Triplett



After \$0F, TLG does an IP bus load. This loads all events into the IP's that will be read out next cycle

The Booster event that was previously loaded (just 18 ms earlier) is now broadcast by the TLG

The non-Booster events that were loaded after previous \$0F are now broadcast by TLG

To make the bmindly pulses:  
 At Bmin, a delay begins via RSTDLY of 64.654 ms.  
 When the delay times out, a bmindly pulse is produced ~2ms prior to Bmin of the following Bmin

Info from Kent Triplett