



MicroBooNE DAQ

Eric Church, Yale
PPD Online Group Meeting
16-April-2014

Outline



- ❑ MicroBooNE Overview
- ❑ MicroBooNE DAQ System Overview
- ❑ System Components
- ❑ Data flow (a story in 9 slides)

MicroBooNE Status



- CD3b March, 2012.
- CD4 by end of 2014
 - MicroBooNE DAQ ready earlier — end of May, 2014
- Electronics Reception Tests have been run and have tested out much of the full DAQ and its moving parts. (Won't report much on those here.)

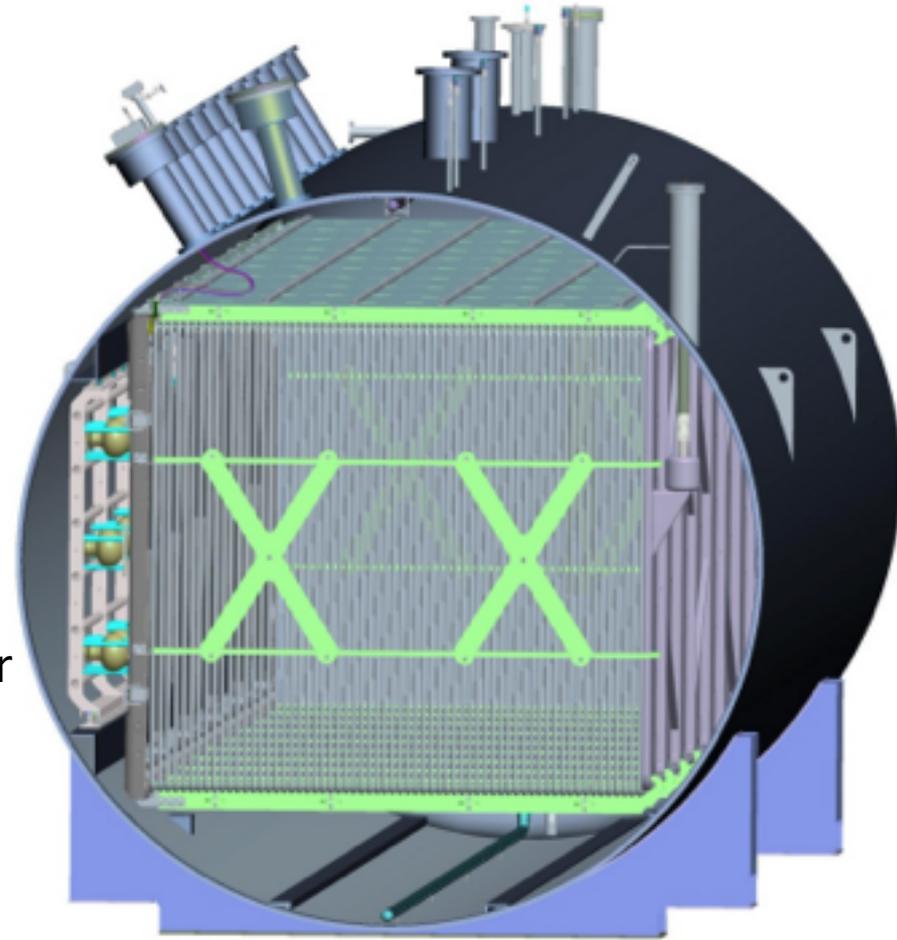
MicroBooNE instrumentation



- 8256 wire channels
- 32+4 PMTs

data on Wires are the projections in 3 views. Allows reconstructing back to 3D tracks and showers.

PMT data to trigger, to determine t_0 for cosmics subtraction, and perhaps late/early light for pID.



The ship goes by almost instantaneously, and you see the flash from the light on its bow; the waves lap up on shore much later.

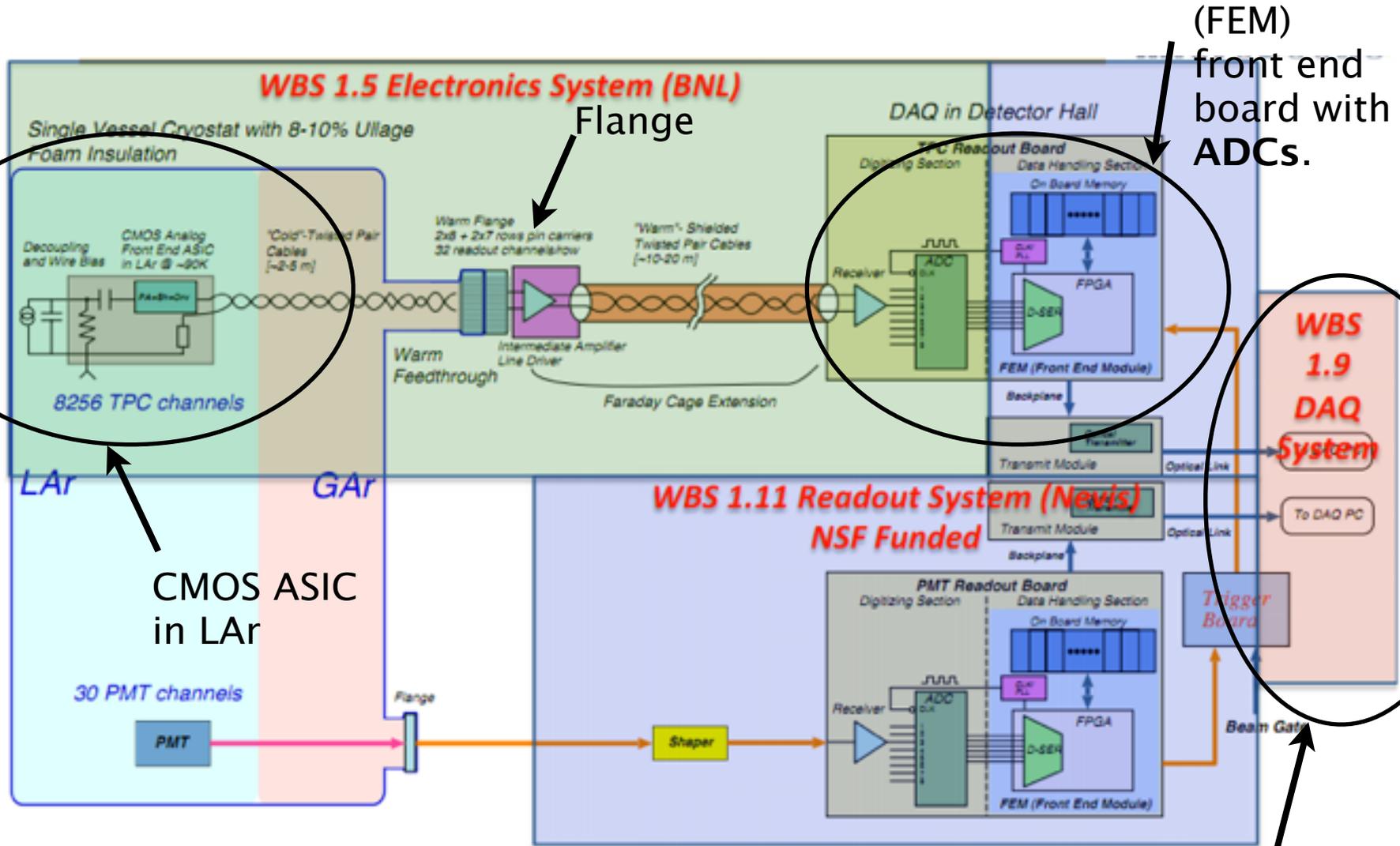
MicroBooNE TPC/Cryostat pictures



16-April-2014

MicroBooNE DAQ Status – PPD Online Meeting

System Overview



(FEM) front end board with ADCs.

CMOS ASIC in LAR

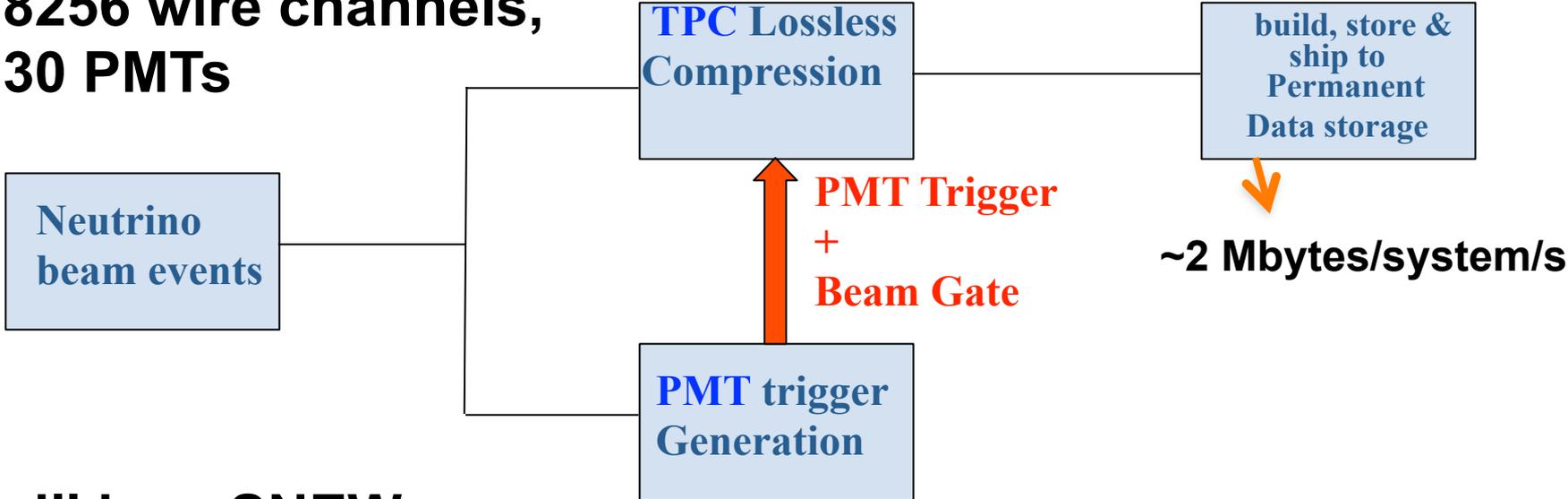
(SEB) sub event buffer

Meeting

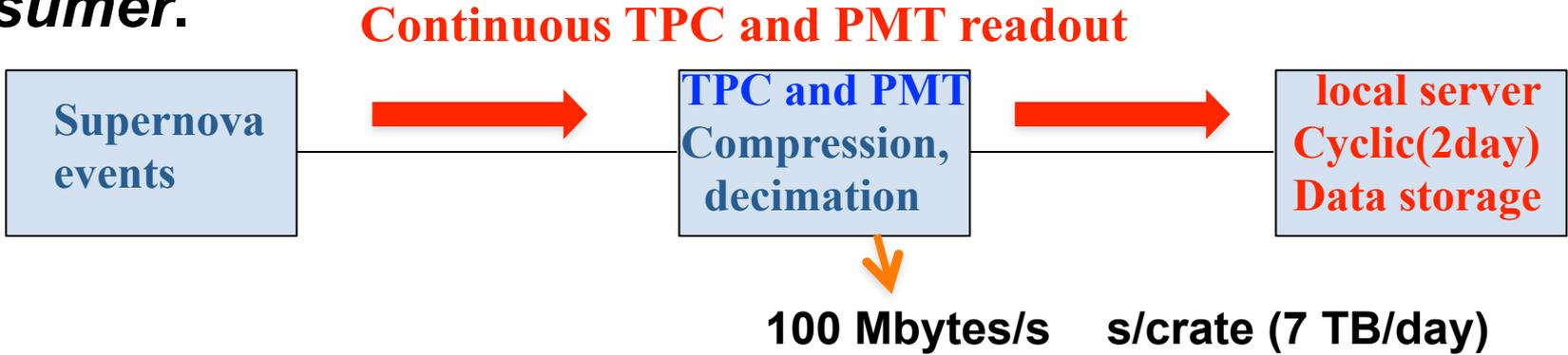
Digitizing Boards: MicroBooNE design



**8256 wire channels,
30 PMTs**



**We will be a SNEWs
consumer.**



2 data streams



- Beam physics: triggered stream
 - confirm/refute/dispute miniBooNE BNB sub-500 MeV excess
 - x-sections in Argon
 - But also: NuMI events
 - Laser calibrations
 - “Strobe” events

- non-Beam physics: Supernova stream
 - Every single 1.6 msec frame, one after the other
 - Will fill seven 2 TB disks in two days on each crate.
 - GPS time of event will allow to dig through and recover 1-2 hrs around the candidate SN, as reported from SNEWS
 - non-trivial disk-read, network-heavy task.
 - data moving, reaping; other bkgd processes always running

Resources



- Work on the DAQ is ongoing at Nevis/FNAL through 2014. Move to LArTF (MicroBooNE enclosure) underway. Computers up and running; electronics will be connected in a final configuration only when the platform over cryostat is finally installed

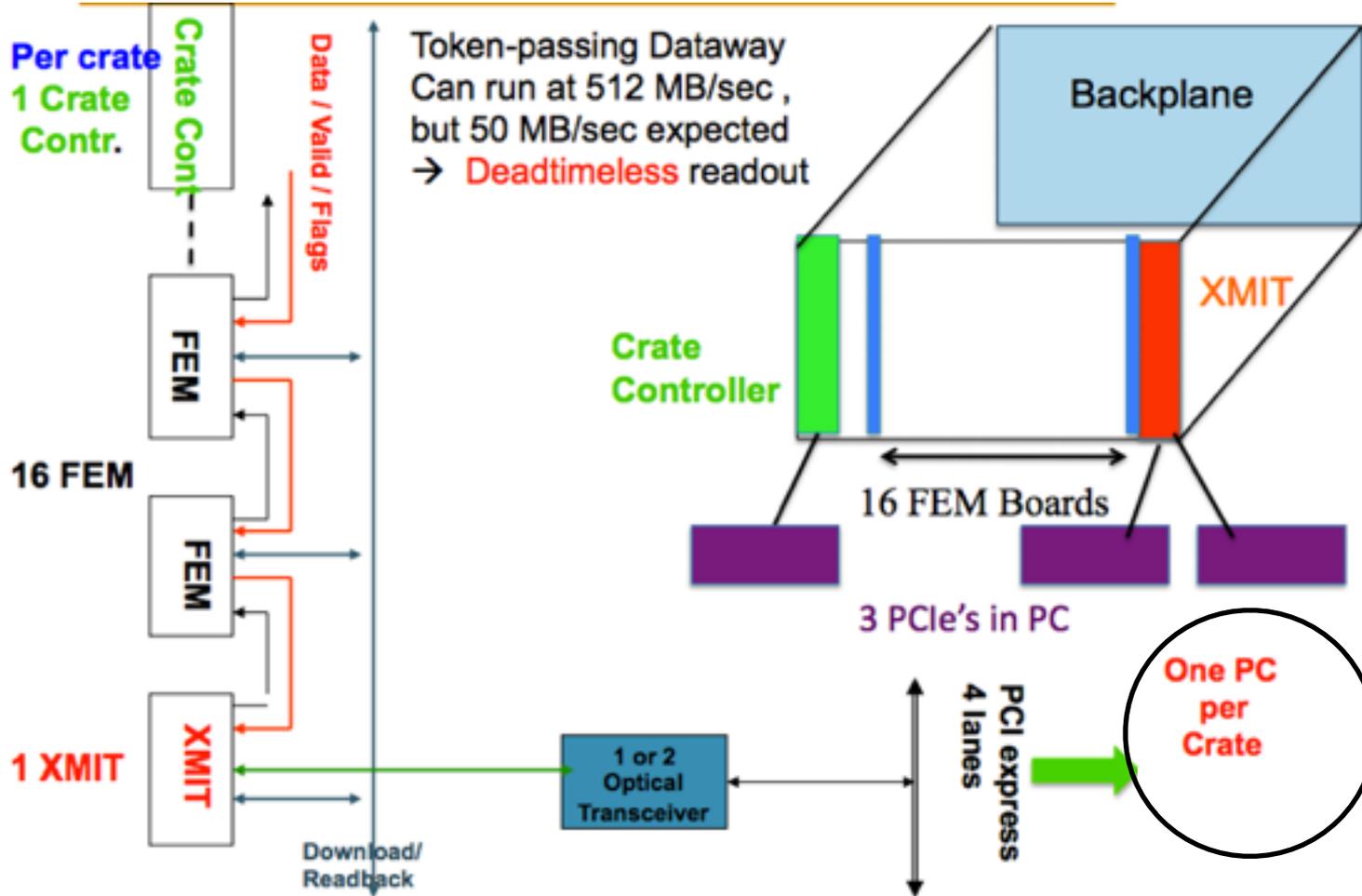
- The MicroBooNE DAQ team is comprised of the following institutions :
 - Yale, LANL, FNAL, Nevis/Columbia, KSU, MIT, Otterbein, VA Tech, UC

uB Test Stands



- There are two Test Stands at DAB.
 - One reads one flange's worth of wires (~960 wires) — MRT
 - charge put on ASICs
 - software trigger
 - One reads 36 PMTs — MRT+
 - pulse flasher diodes
 - external trigger
- This has been halted for now while TPC construction is finalized

Nevis TPC Crates (x9)



Wires are sampled @ 2MHz, 2 bytes

Fibers into SEB-computers



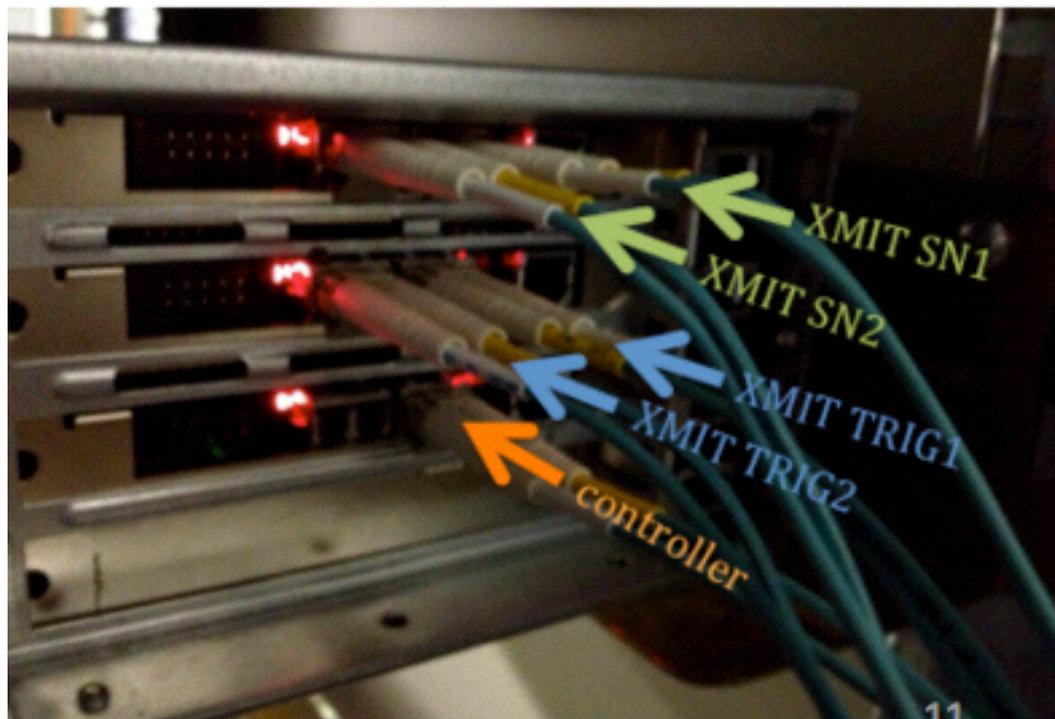
SEB == Sub Event Buffer <==> basically one crate.

One SEB computer services one crate.

There are two data streams.

- (1) Triggered
- (2) Supernova:
continuous stream

Both come through
the "XMIT" card on
duplex fibres.



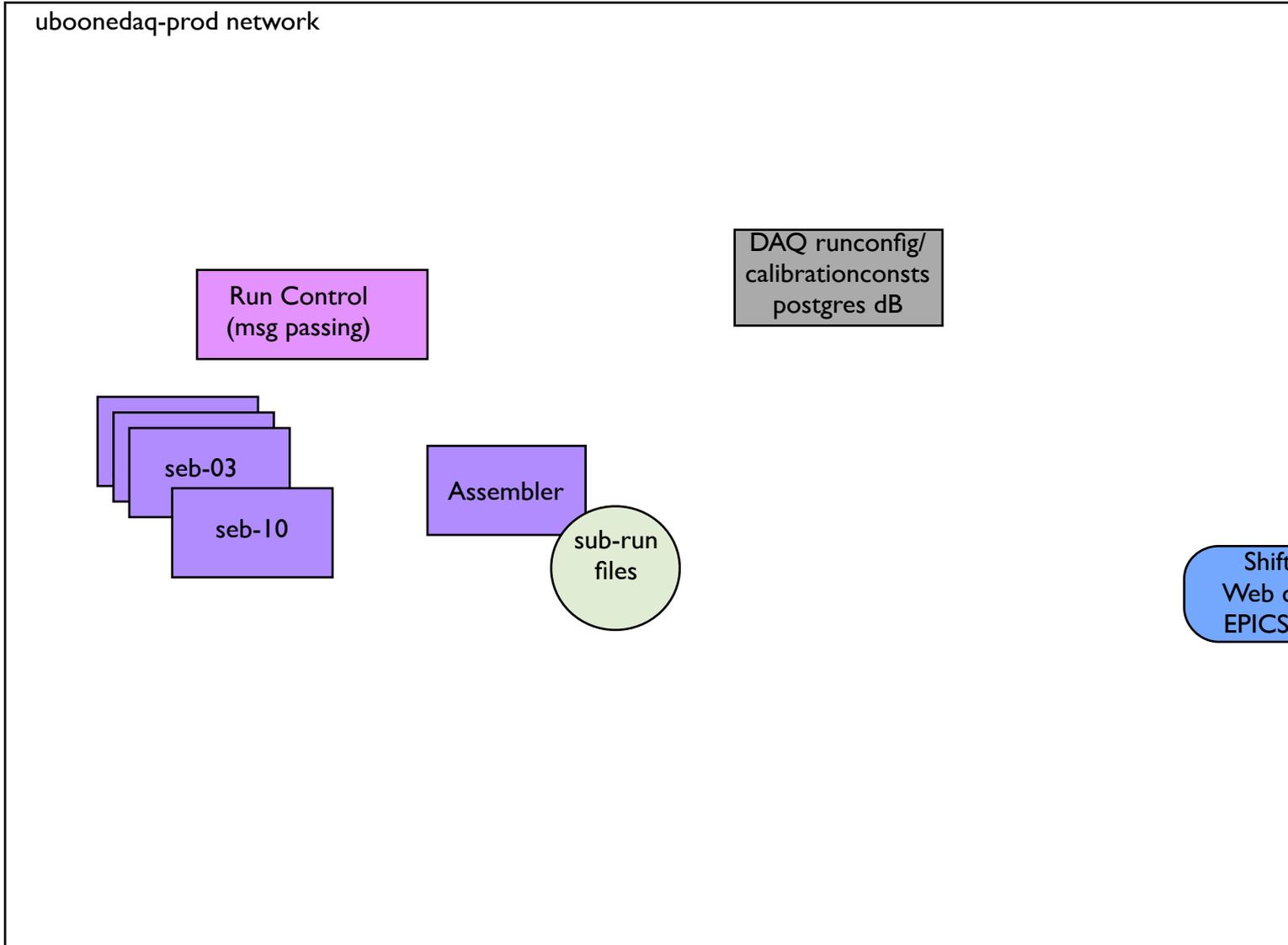
Three NEVIS custom PCIe cards per SEB.

Overview of DAQ Project

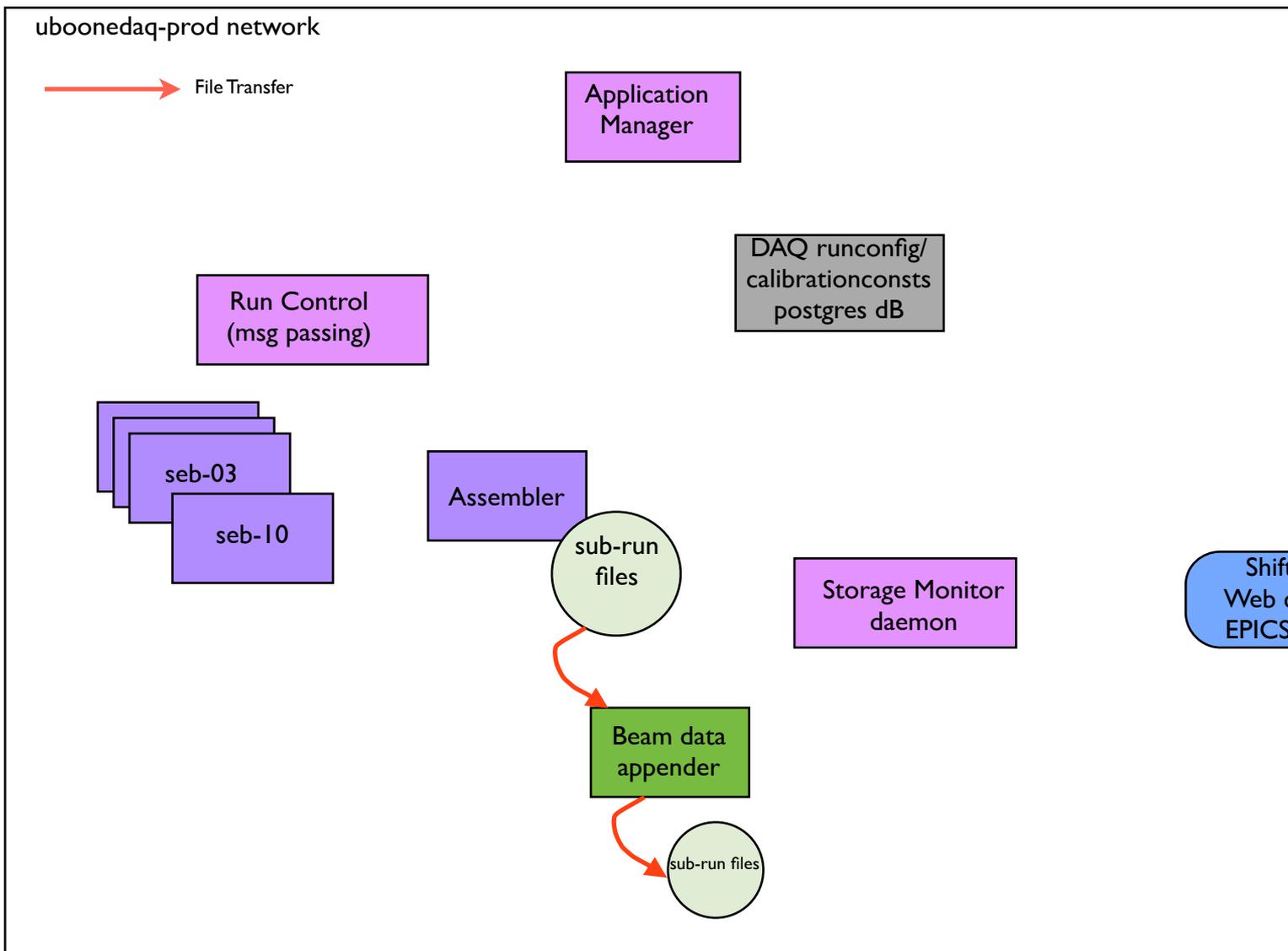


- The MicroBooNE DAQ is responsible for reading out, assembling events, writing them to file.
- But also:
 - Monitoring and Control: EPICS database
 - Beam data concatenation
 - Online monitoring
 - Run Control
 - Calibration runs, Laser Runs, Regular runs ...
 - Swizzling (DAQ binary to ART ROOT format)
 - DAQ dB and interaction with Offline dB
 - File management, ...

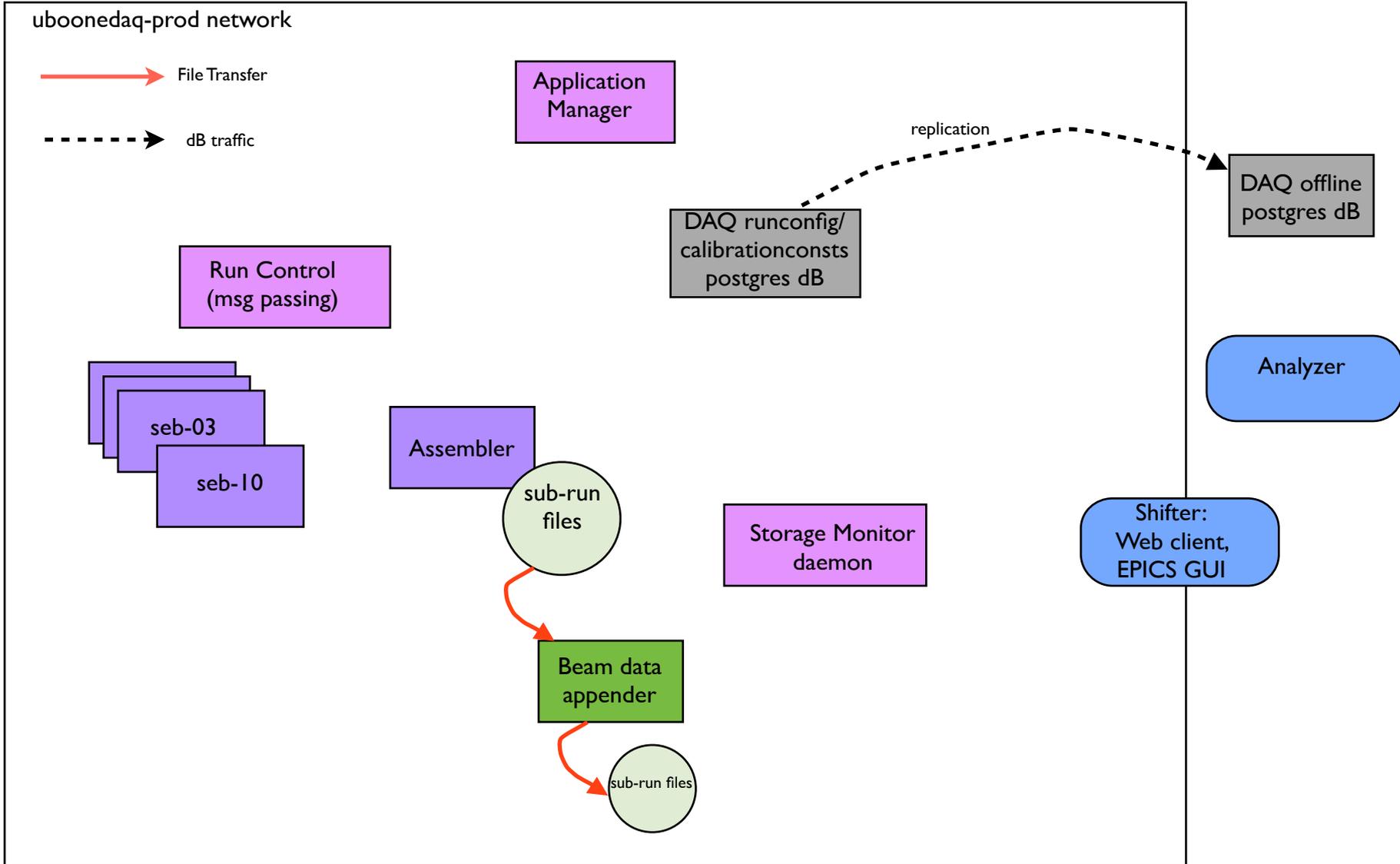
Online/Offline DAQ systems



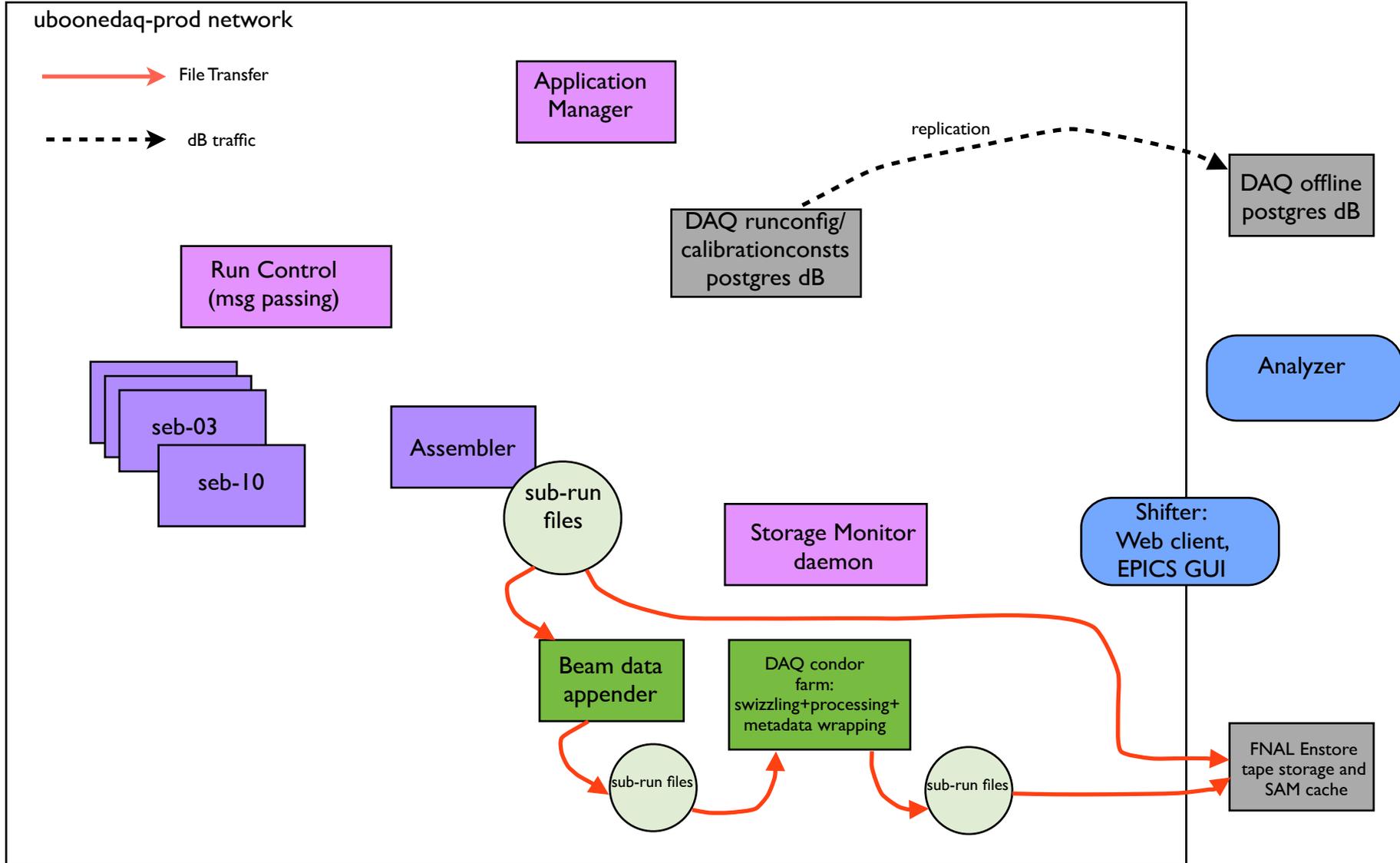
Online/Offline DAQ systems



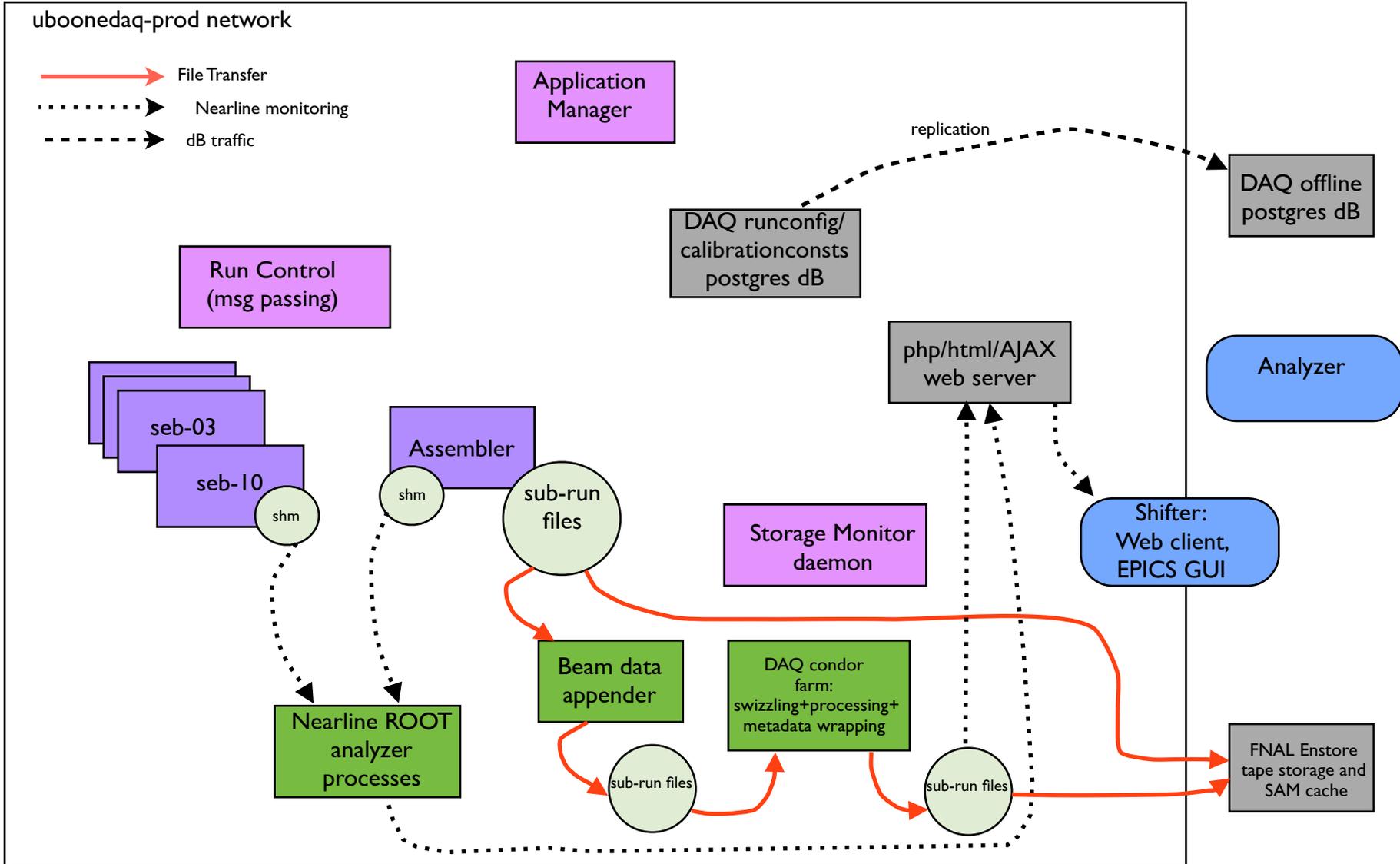
Online/Offline DAQ systems



Online/Offline DAQ systems



Online/Offline DAQ systems

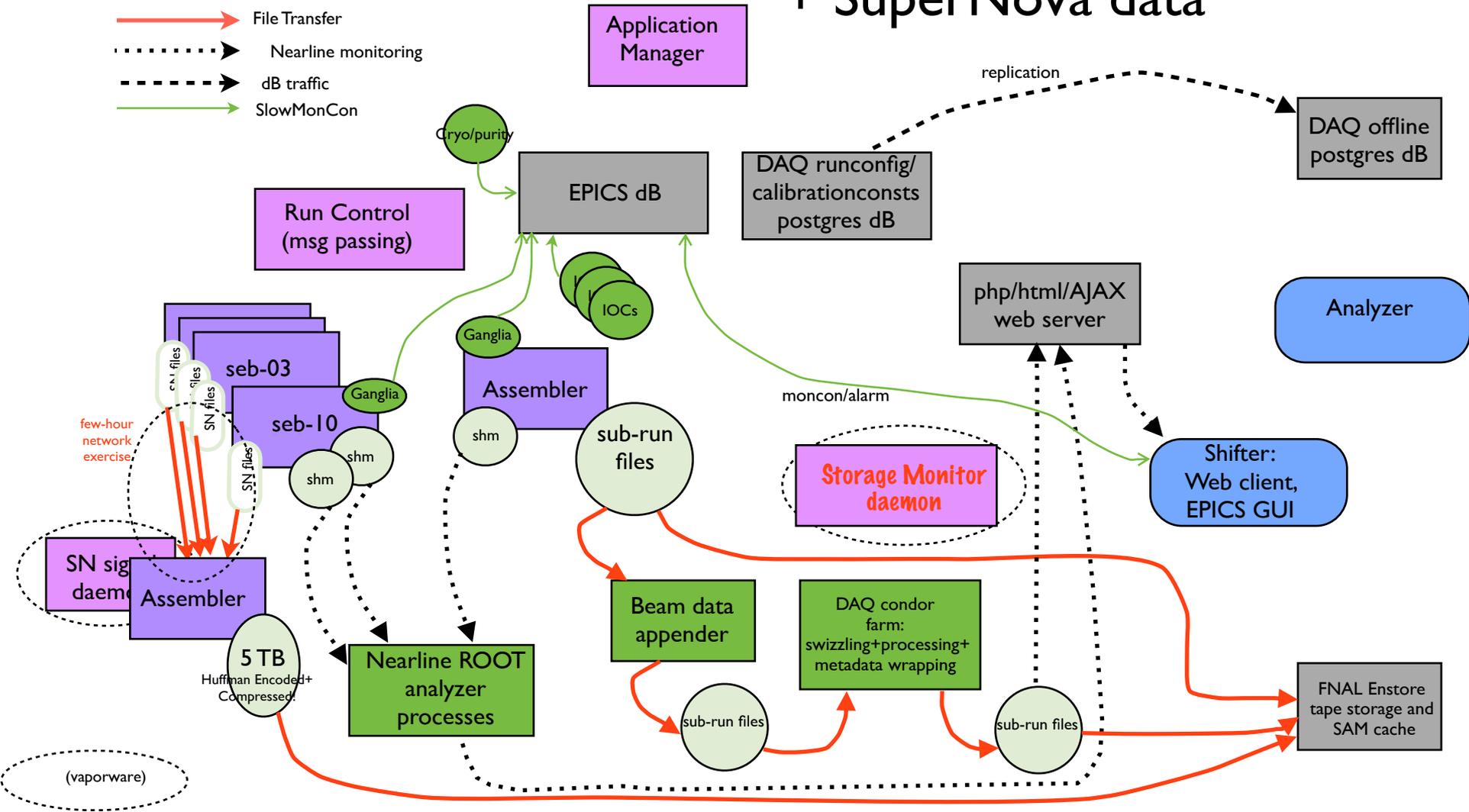


Online/Offline DAQ systems

uboonedaq-prod network

+ SuperNova data

- File Transfer
- Nearline monitoring
- dB traffic
- SlowMonCon



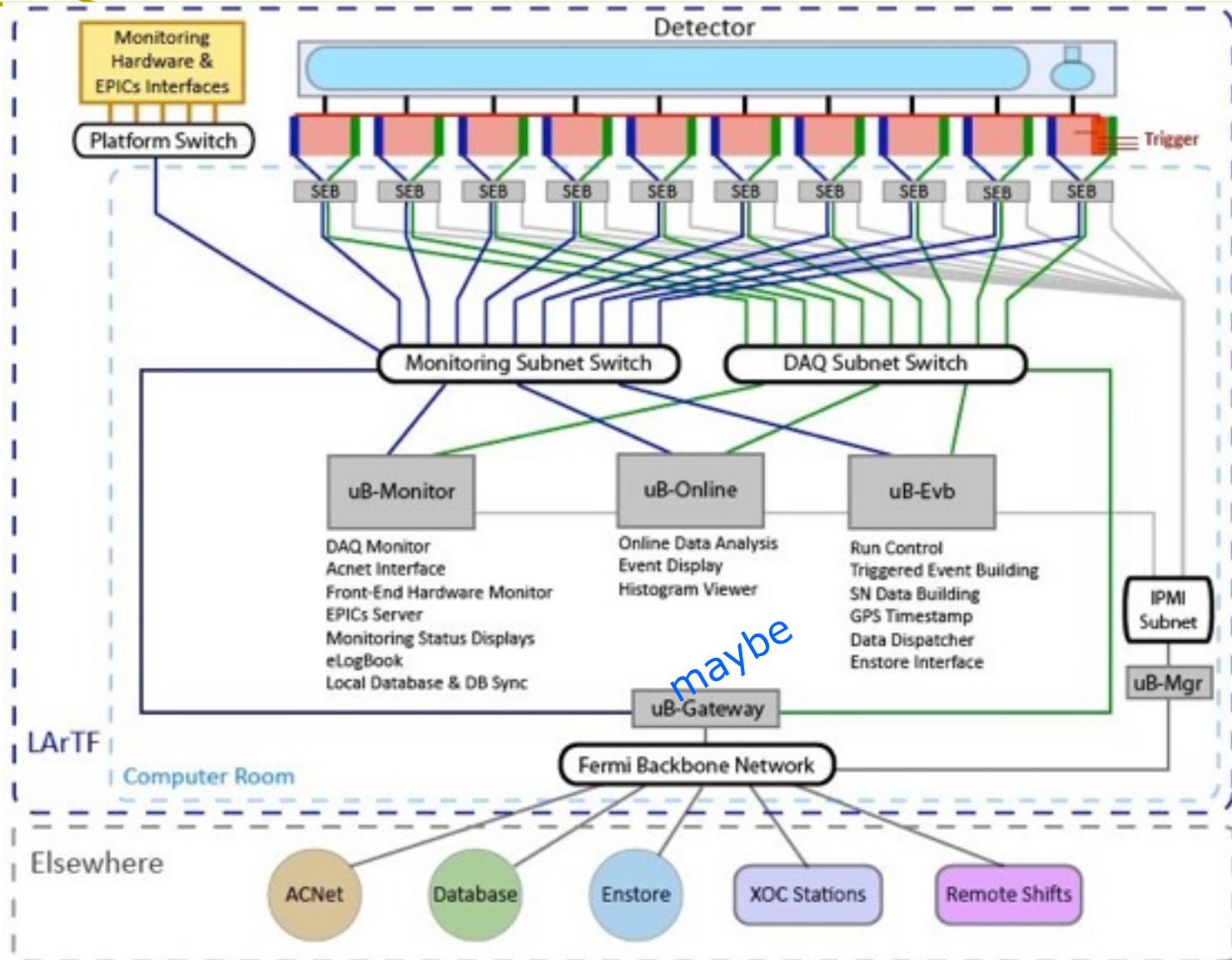
Summary

- All the DAQ moving parts are accounted for and in mature development or complete.
- (Will be) Ready for turn-on and data-taking in 2014
- Exciting times for MicroBooNE!
- Good instructions and pre-commissioning (May 29, 2014) list of tasks at <https://cdcv.s.fnal.gov/redmine/projects/ubooneDAQ/wiki>

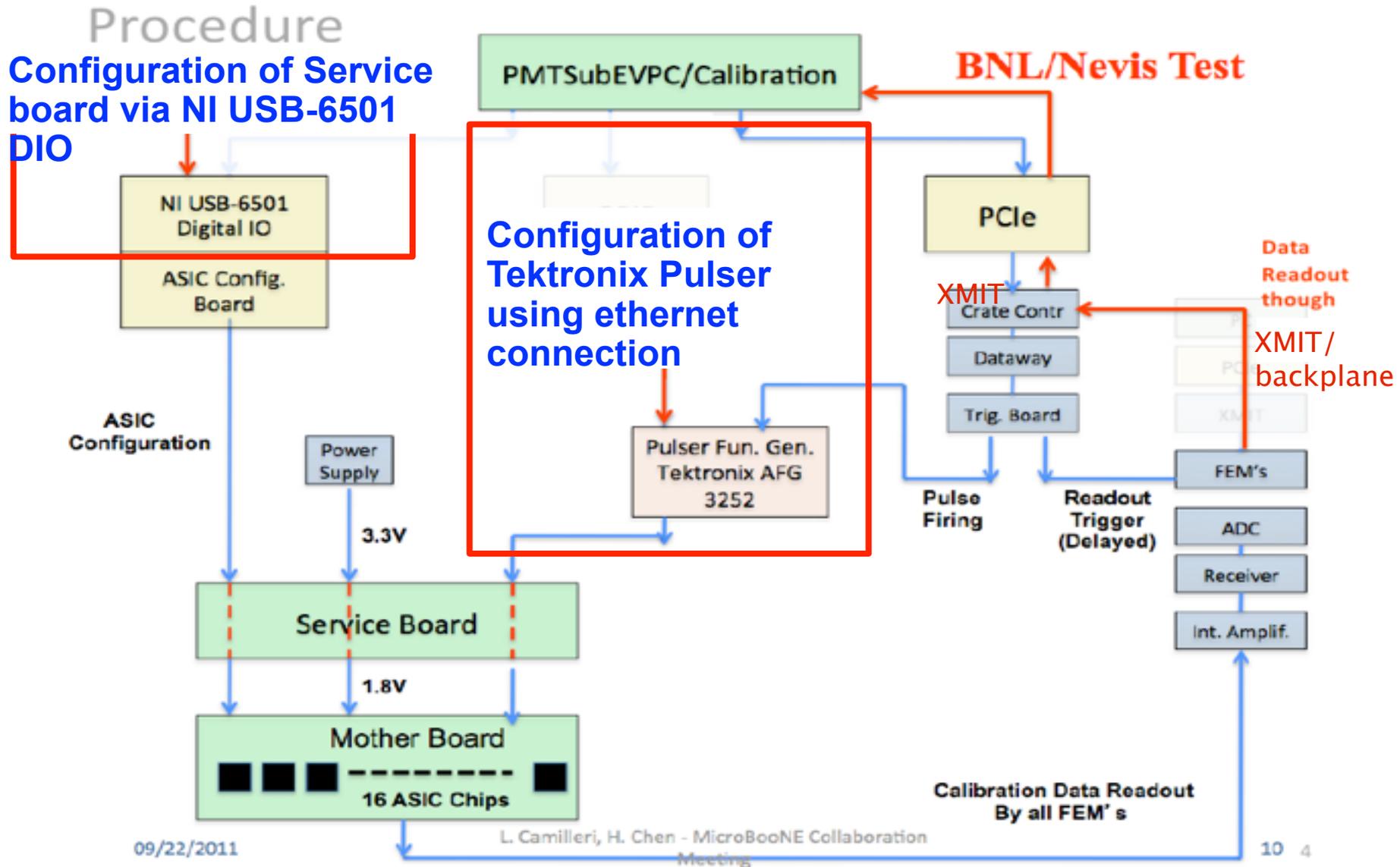
Backup Slides



DAQ Network/Process Overview

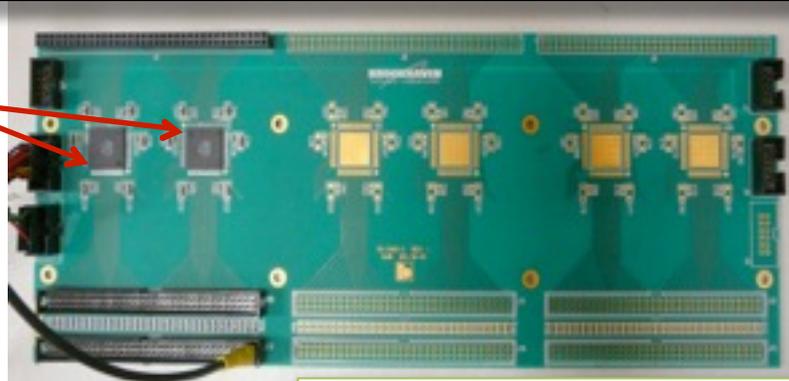
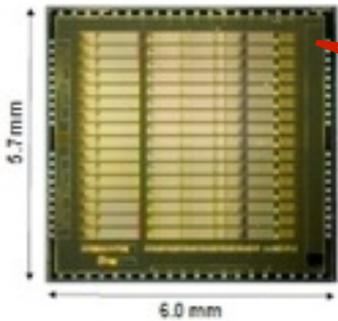


Calibration Hardware



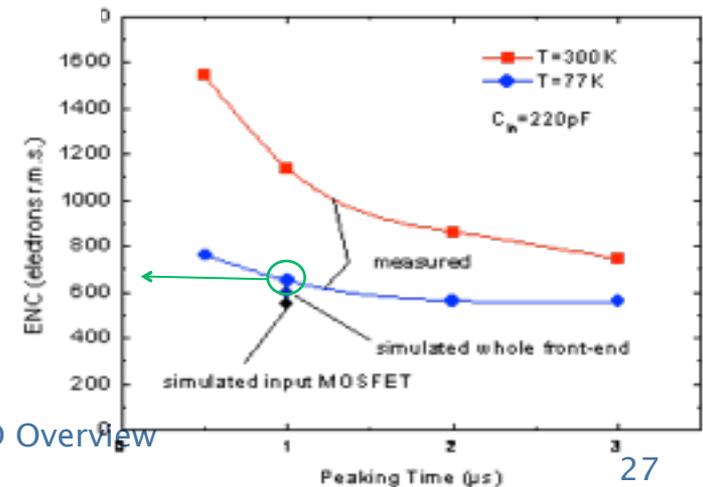
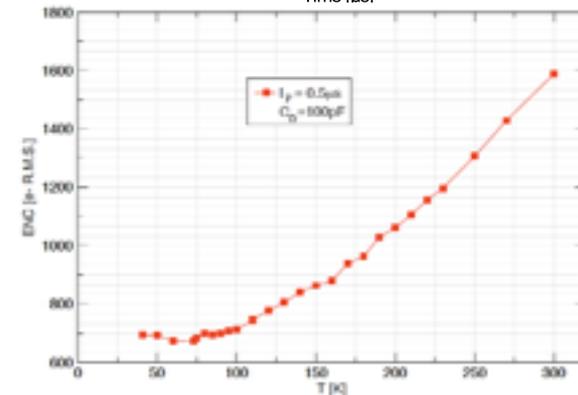
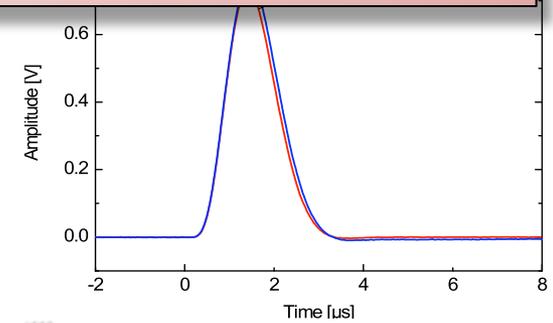
Cold CMOS Analog Front End ASIC & Motherboard

ASIC die & package



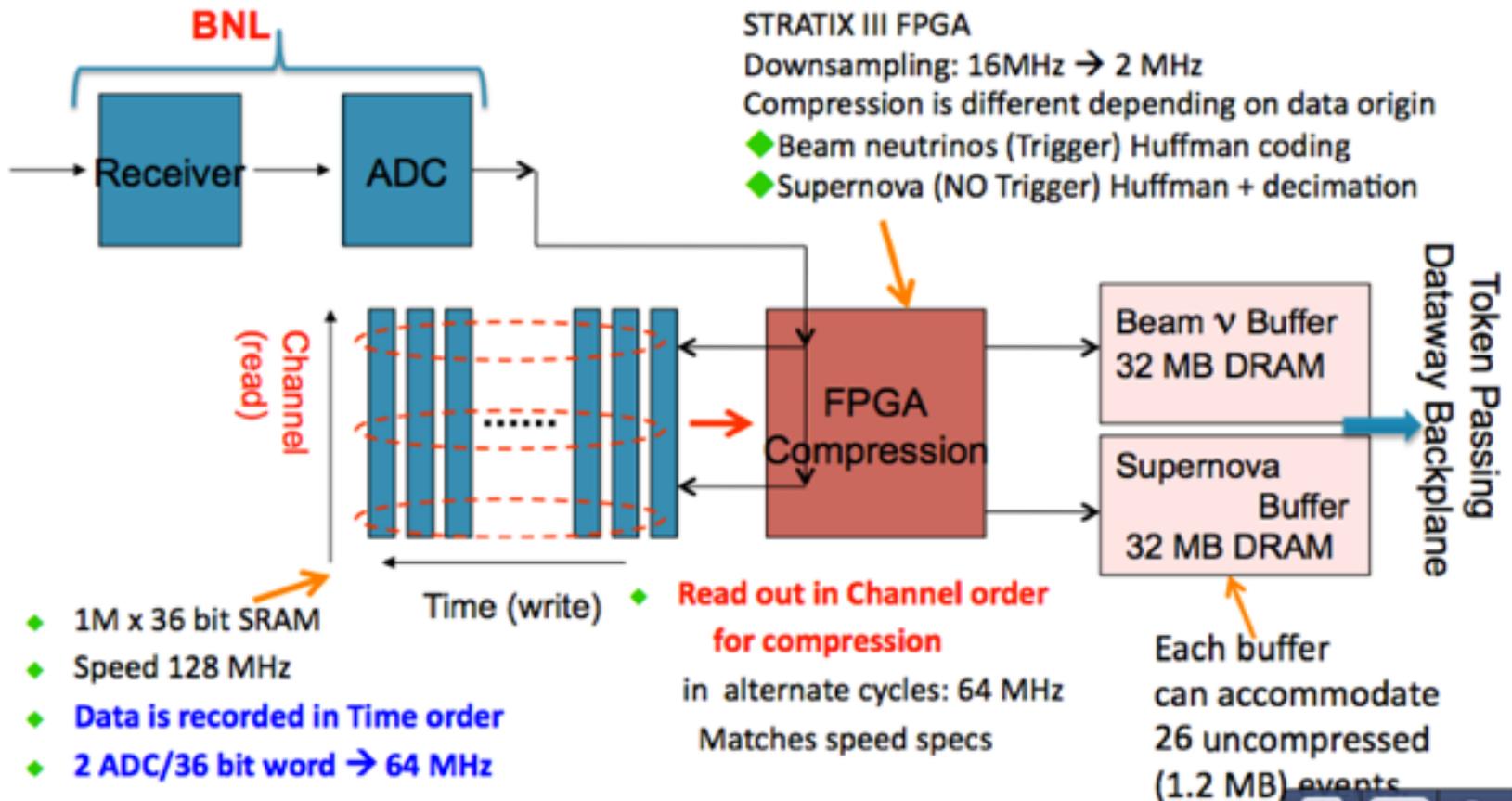
Cold motherboard with 12 ASICs chips (2 shown)

- 16 channels per chip
- Charge amplifier, high-order filter
- Adjustable gain: 4.7, 7.8, 14, 25 mV/fC (55, 100, 180, 300 fC)
- Adjustable filter time constant (peaking time): 0.5, 1, 2, 3 μ s
- Selectable dc/ac (100 μ s) coupling
- 136 registers with digital interface
- 5.5 mW/channel (input MOSFET 3.6 mW)
- Designed for long cryo-lifetime
- Circuit performance is almost identical at 300K and 77K, except noise is \sim 2x lower
- Calibration capacitor on ASIC changes by \sim 0.5% from 300K to 77K
- **Cycle #4* chips: Passed all tests**

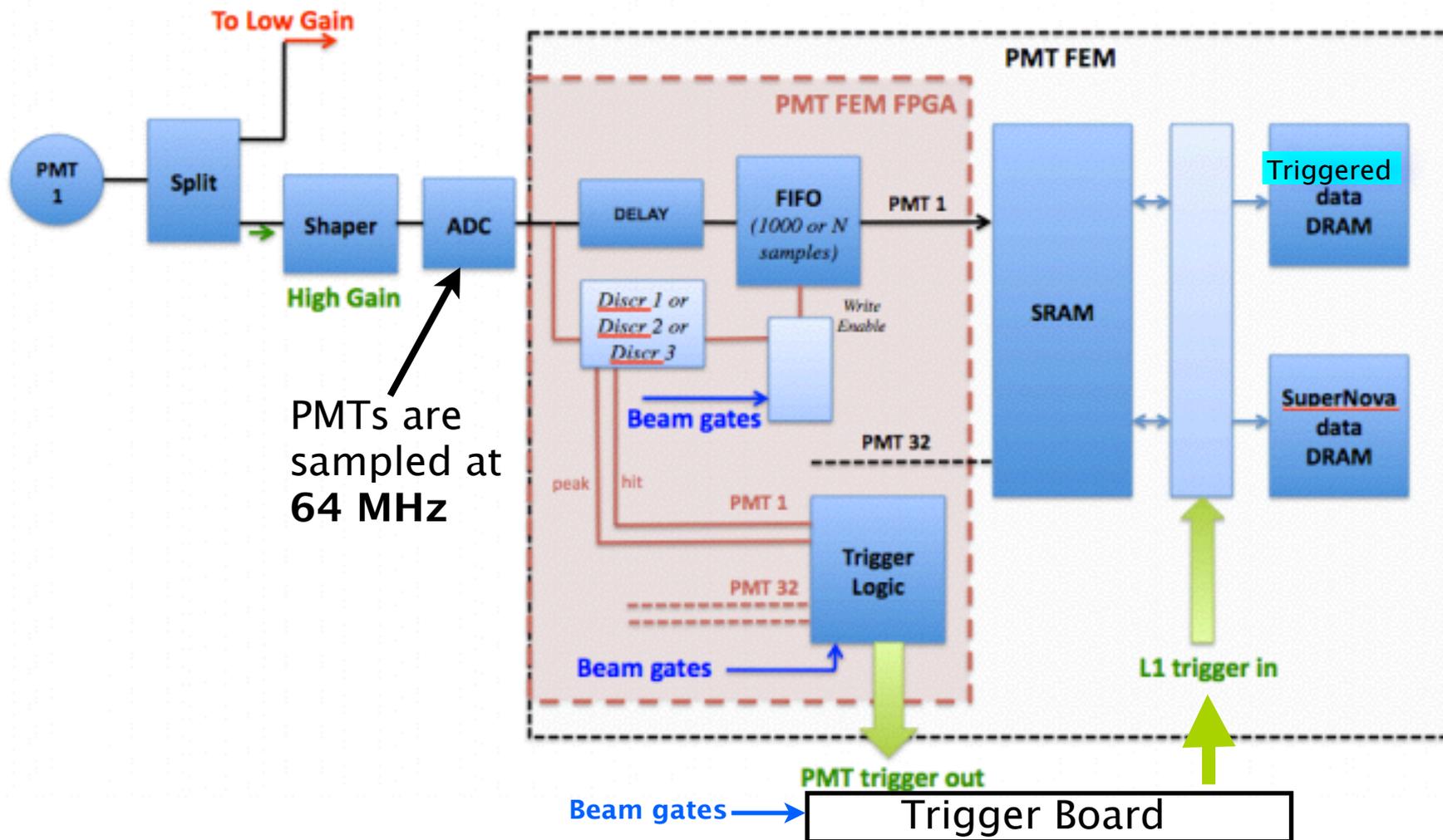


Overview: Digitizing Boards: Hardware and Tasks

Continuous Data rate per card: 64 wires x 2 MHz = **128 MHz** 12 bit ADC words.



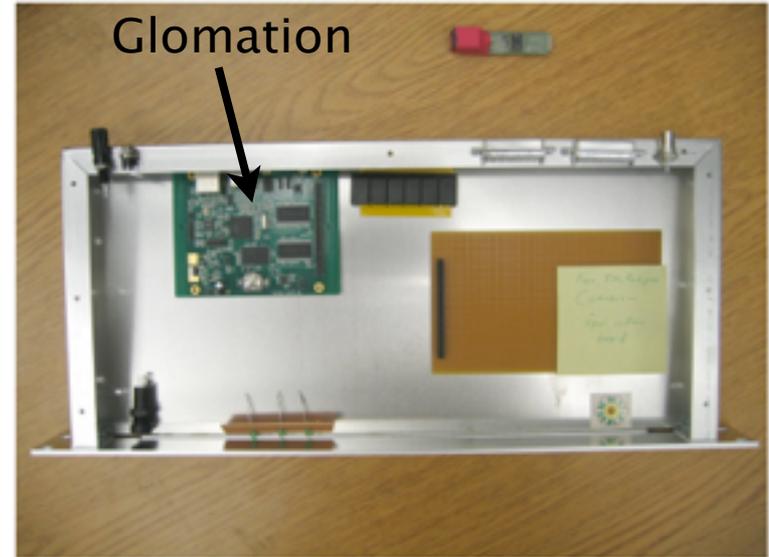
Trigger



Glomation Single Board Computer GESBC-9G20



- SBC includes
 - Linux OS
 - Ethernet
 - RS232
 - USB
 - 40 digital I/O
 - 4 ADC
 - I2C and SPI bus



- Interfaces directly with
 - **Glassman Drift HV – RS232**
 - **Rack Temperature – I2C bus using Maxim DS1624**
 - **Rack Fanpack – digital I/O**

Glenn Horton-Smith, KSU