

# MicroBooNE TPC Crate Tests

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## Abstract

*In order to commission the TPC readout equipment, exhaustive tests were run on each individual board, each fully loaded backplane and all final crate configurations. Readout tests were performed through both controllers and XMITs, and, in the case of the XMITs, both neutrino and supernova streams. All problems encountered during the course of testing were fixed and further tests were conducted before final commissioning of each crate. As of August 7, eight out of nine TPC crates are fully commissioned. Four of the eight have been sealed and shipped for installation at PBC. The other four will be shipped shortly. The final crate is being withheld temporarily for diagnostic tests on the DMA timeout errors.*

## I. INITIAL INVENTORY, INSPECTION AND FINAL ASSEMBLY OF BOARDS

After being received from the assembler, all boards were visually inspected by Nancy Bishop and Cheng-Yi Chi. Additional components were mounted on the boards as needed by Nancy Bishop. The nomenclature for referring to the serial numbers of boards (whose locations are labeled in the aforementioned figures) are:

- “FEM001” for Nevis serialized front end module number 001 (Figure 1)
- “ADC001” for BNL serialized 9U TPC ADC number 001 (Figure 1)
- “CTRL01” for Nevis serialized controller board number 01 (Figure 2)
- “XMIT01” for Nevis serialized XMIT number 01 (Figure 3)
- “TRIG01” for Nevis serialized trigger board number 01 (Figure 4)
- “BKPL01” for Nevis serialized crate backplane number 01 (Figures 5 and 6)
- “CLCK01” for Nevis serialized clock module number 01 (Figures 7)
- “CLCKF01” for Nevis serialized 6U clock fanout number 01(Figure 8)

The Nevis FEMs were tested both on their own and after being mated with a Brookhaven ADC board. Separate ADC board tests were conducted by Brookhaven. A picture of a mated “ADC+FEM” board is shown in Figure 1.

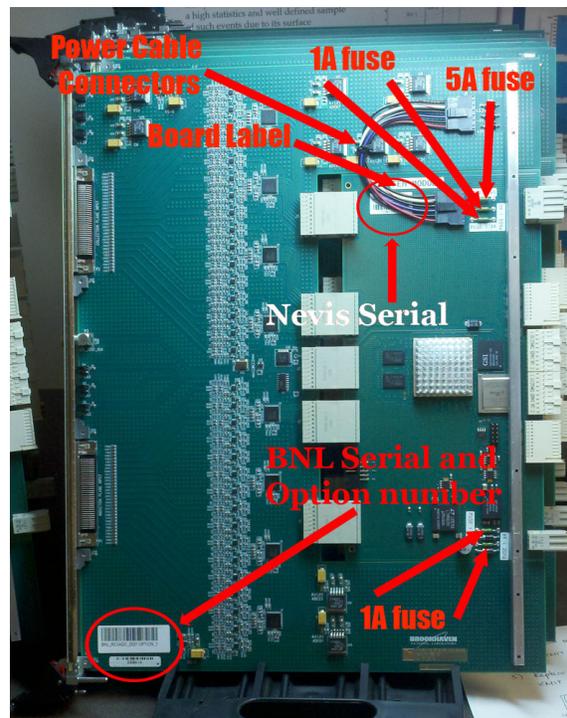


Figure 1: A mated TPC ADC(BNL) + FEM(Nevis) board

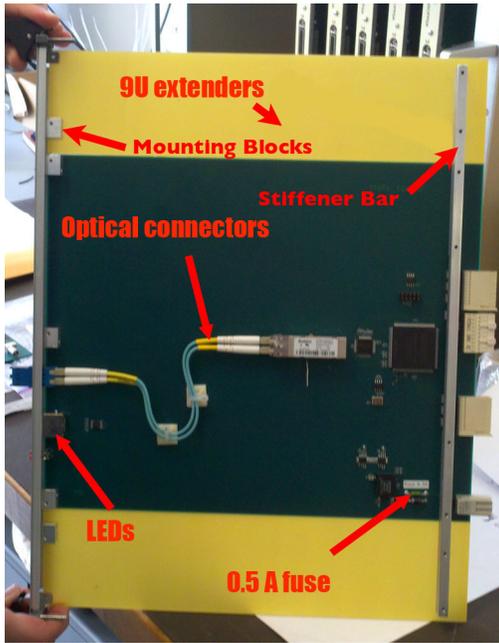


Figure 2: Controller board (CTRL)

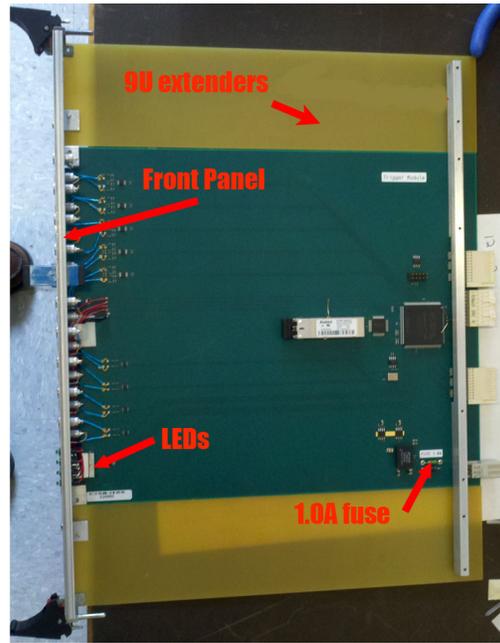


Figure 4: Trigger board (TRIG)

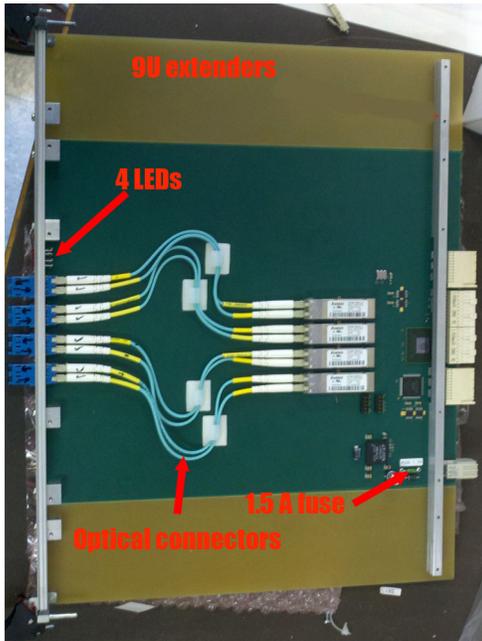


Figure 3: XMIT board with 9U extenders

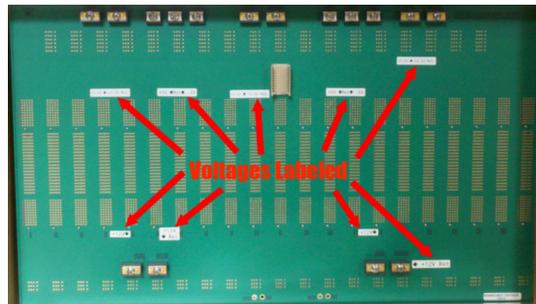


Figure 5: Backplane (BKPL). Note: Nevis serial-izatin is missing

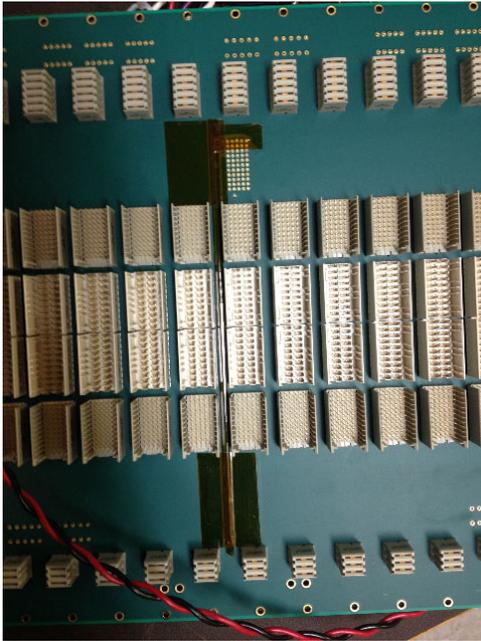


Figure 6: Front side of a backplane. Note the covering of 12V trace with Kapton tape

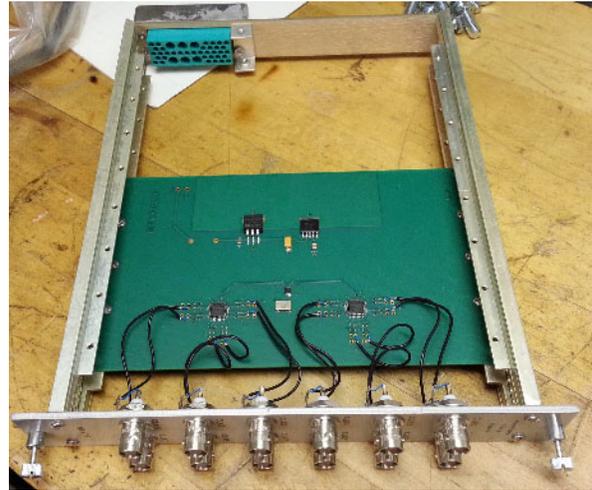


Figure 8: Clock fanout (CLCKF)

## II. INDIVIDUAL BOARD TESTS

The following individual board tests were completed in spring 2013 and more extensive procedural documentation is available in "Production Tests for MicroBooNE Electronics". The results shown here are meant to provide a concise summary.

### II.1 Front End Module (FEM) and ADC+FEM Tests

All 147 FEMs were individually tested by connecting each board into a 6U crate and confirming backplane power connections by taking readings at particular voltage test points. Firmware was then loaded onto each FEM and the board was booted to verify success.

The first test performed involved slow readout through the controller. In order to check FEM booting, FPGA configuration and DRAM memory integrity, 1,000 fake events were generated with the Stratix III and their consistency was checked after readout.

All FEMs passed this test. However, a couple issues were observed and later resolved. The first dealt with bad header data. This was fixed by repairing the eprong on the faulty board. The second was data mismatch. This was likely



Figure 7: Version 4 of a clock module (CLCK). Note that the serial number is missing

because the wait times between the trigger and readout were too short.

These results are summarized in Figure 9.

FEM #	Issue #
FEM015	1
FEM018	1
FEM019	1
FEM023	1
FEM025	2
FEM028	1
FEM029	1
FEM030	1
FEM033	1
FEM034	1
FEM041	2
FEM042	2
FEM045	2
FEM046	2
FEM047	2
FEM068	2
FEM084	1
FEM096	2
FEM116	2
FEM117	2

Figure 9: FEM slow readout test results. Issue 1 corresponds to bad header data, while issue 2 corresponds to a data mismatch

In the second test, readout occurred through the XMIT Trigger path readout with 20,000 randomly generated fake events submitted for data checking. The FEMs being tested (>10 at a time) were sandwiched between two working prototype FEMs. The goals were to check the memory integrity, backplane links and token passing within each board.

All FEMs again passed this test, with the exception of a few FEMs that showed two problems. The first issue was a direct memory access (DMA) timeout. This problem will be discussed extensively below in the section V of this write-up.

The second issue was bad data readout from the board. In the offending boards, one or two bits were wrong in many channels. This issue was found to be temperature dependent and was solved by installing heat sinks on the FPGAs of all boards. These results are summarized in Figure 10.

FEM #	Issue #
FEM041	1
FEM057	2
FEM137	1
FEM146	1

Figure 10: FEM XMIT readout test results. Issue 1 corresponds to DMA timeouts, while issue 2 corresponds to a data mismatch

The next test involved readout through the XMIT supernova channel. The setup was identical to the previous test, except only 1 or 2 FEMs were tested at a time. The goals were again to check memory integrity, the backplane links and the token passing scheme.

All FEMs passed this test. Some boards had DMA timeout errors, but all eventually passed the test when run repeatedly. The source of these errors will be discussed in section V.

After the FEMs were all individually tested, they were mated to BNL-produced ADCs and tested together in a 9U crate. Slow readout was then tested with real calibration data. Three boards were used at a time and baseline and linearity data were extracted.

## II.2 Controller Tests

Each controller was tested with data loopback, speed, single FEM boot and slow readout tests. All controllers passed the tests; no issues were observed. The results are summarized in Figure 11.

Serial	1FEM Current (A)	Loopback	Speed: 2 kWords(MB/s)	Speed: 1kW	Slow Readout
CTRL01	0.597	ok	6.027	5.431	ok
CTRL02	0.595	ok	6.023	5.430	ok
CTRL03	0.608	ok	6.023	5.410	ok
CTRL04	0.608	ok	6.036	5.440	ok
CTRL05	0.606	ok	6.034	5.440	ok
CTRL06	0.601	ok	6.036	5.450	ok
CTRL07	0.603	ok	6.034	5.440	ok
CTRL08	0.600	ok	6.036	5.430	ok
CTRL09	0.598	ok	6.029	5.440	ok
CTRL10	0.597	ok	5.975	5.400	ok
CTRL11	0.598	ok	5.976	5.400	ok
CTRL12	0.595	ok	5.976	5.400	ok

Figure 11: Controller test summary. "1FEM Current" means current reading at boot time with only 1 CTRL and FEM in the Crate

### II.3 XMIT Tests

XMIT tests were performed to verify the booting process and the neutrino and supernova path readouts. All XMITs passed these tests, although a couple XMITs had DMA timeout errors in the supernova stream. The results are summarized in Figure 12.

Serial	Boot OK?	Data Mismatch? ( $\nu$ /SN)	DMA timeout? ( $\nu$ /SN)
XMIT01	yes	no/no	no/yes, several. Last run OK
XMIT02	yes	no/no	no/no
XMIT03	yes	no/no	no/no
XMIT04	yes	no/no	no/no
XMIT05	yes	no/no	no/no
XMIT06	yes	no/no	no/no
XMIT07	yes	no/no	no/no
XMIT08	yes	no/no	no/no
XMIT09	yes	no/no	no/no
XMIT10	yes	no/no	no/no
XMIT11	yes	no/no	no/yes, several. Last run OK
XMIT12	yes	no/no	no/no

Figure 12: Summary of XMIT tests

### III. BACKPLANE TESTS

Backplane tests were conducted to ensure proper connections between the board and backplane in each slot of the crate. It also served to test the upper limit of how many boards the voltage settings and token passing scheme could service.

Before each backplane test, voltage points were tested in an empty crate to make sure they matched expectations. This was done to prevent damage to boards from any improper voltage setting. Voltage and current readings were made at multiple points during this process and those readings are available in Appendix B.

The crate was then fully populated with 18 ADC+FEM boards, with a crate controller in the second slot from the left and the XMIT in the farthest slot to the right. Fake data was loaded onto the FEMs and at least 50,000 events were readout and checked against the initial word. Data during this initial test was read out through the trigger path.

All boards booted properly and passed this test, however a few boards had persistent DMA timeout errors. These results are summarized in Figure 13 (and DMA timeout errors are discussed below).

Board	Slot
FEM19	5
FEM33	16
FEM56	
FEM63	
FEM94	

Figure 13: Particular crates and slots that caused DMA timeout errors

The next test used the same board configuration, but this time read out was through the supernova path. As such, only four boards were read out at a time to minimize the amount of data written to the DAQ machine (since only one ASIC motherboard was available). The configuration for the first two full crate configurations are shown in Figures 14 and 15.

All boards passed this test, except FEM33. FEM33 had several data mismatches that got progressively worse with time. This was likely an isolated, temperature dependent event, since FEM33 later passed this test with no further problems.

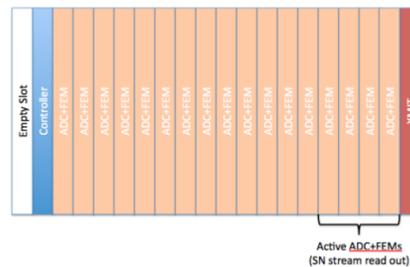


Figure 14: Crate setup for the supernova backplane test, first configuration

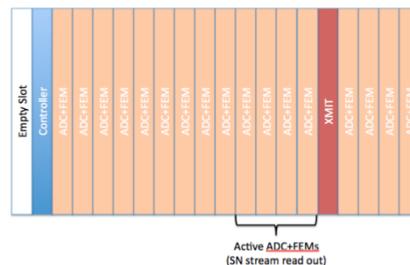


Figure 15: Crate setup for the supernova backplane test, second configuration

#### IV. FINAL ASSEMBLY TESTS

The final assembly tests were designed to test the final crate configurations to be used in MicroBooNE. By this point, all individual components were tested, and this served as a final check against any unforeseen problems using real data. To simulate the conditions of the actual experiment an analog signal from a function generator was sent through the trigger board and into the FEM/ADCs. There the signal was digitized, condensed and stored.

In the first set of tests, data was then read out through the controller; in the second, it was read out through the XMIT. All crate configurations passed these tests. Boards booted properly, data integrity was maintained, pulses and proper baselines were observed in all channels and input voltage and output ADC values remained linear until saturation.

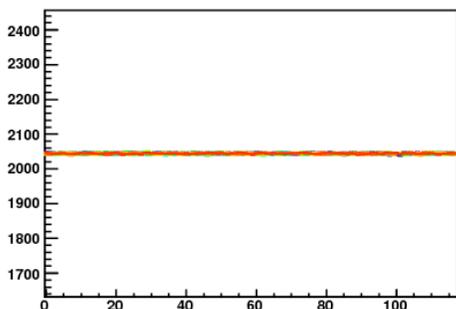


Figure 16: At 0 V, a pulse is not visible, as expected

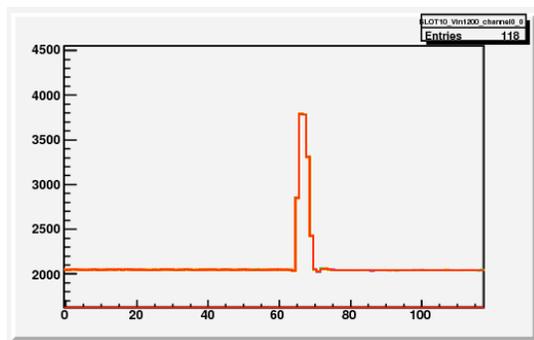


Figure 17: At 1200 V, on the other hand, a pulse is expected and observed across all boards

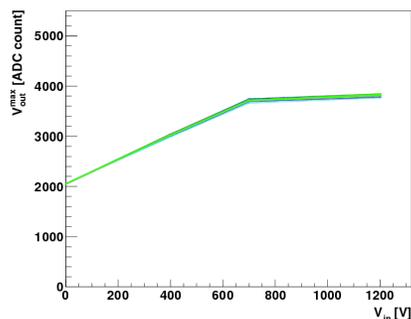


Figure 18: The relationship between input voltage and output ADC should be linear. If it were not, output data would have been somehow corrupted. All channels of all boards, were correct. From this plot, all 64 channels of this particular FEM/ADC have a proper baseline. This result was consistent for all boards across all such tests.

#### V. DMA TIMEOUT ERRORS

DMA (direct memory access) timeout errors refer to an exception thrown during the read out process of a particular event. Under the token passing scheme, data is passed in small batches to the XMIT from one particular board at a time. It is then written directly to the DAQ machine without tying up computer CPU. When a DMA timeout error is observed this process hits a roadblock, with a batch of data stuck in the XMIT and never getting written to DAQ. This halts the token passing process and the testing algorithm throws an exception.

These type of errors initially appeared during the testing of individual boards. A number of solutions were proposed and implemented with varying degrees of success. The most successful appeared to be reinstalling firmware on the boards. However, the problem reappeared during the backplane tests with fully loaded crates.

This time around we were able to isolate the problem to particular boards in particular slots across multiple crates. If either the slot or board was changed, the problem could be suppressed. Upon returning to the problematic configurations, DMA timeout errors were

always observed if enough events were processed; it usually took between 5,000-20,000 events to observe a DMA timeout.

Fortunately, we witnessed a DMA timeout occur at the same moment that a fan in the same crate as our clock was shut off. This gave us the idea of trying to induce a DMA timeout by turning on and off the fan. Incredibly, almost every time the switch was flipped a timeout was immediately induced. Upon attaching a scope to the clock we were able to witness a voltage spike at the moment the fan's power switch was flipped. Furthermore, by connecting a surge protector to the common power source we were able to eliminate the problem. Long runs of 200,000 events were taken with no errors and our method of inducing errors no longer worked.

Further diagnostic tests are being performed on the final crate (the only crate to have problematic boards) in order to fully understand this problem. It will be important to understand why these errors only afflict particular boards.

## VI. CRATE STATUS (AUGUST 7, 2013)

As of August 7, the status of each of the nine crates can be seen in Figure 19. In Figure 20, the four crates just shipped are shown sealed and wrapped for delivery.

Crate	Status
1	Shipped
2	Shipped
3	Shipped
4	Shipped
5	Ready to ship
6	Ready to ship
7	Ready to ship
8	DMA timeout diagnostic testing
9	Ready to ship

Figure 19: Current status of each individual TPC crate



Figure 20: Four crates sealed before being shipped

## VII. APPENDIX A: FINAL CRATE CONFIGURATION

Crate 1		Option	Notes
CTRL11			
FEM105	ADC139	2	
FEM106	ADC134	2	
FEM116	ADC146	2	
FEM108	ADC131	2	
FEM109	ADC124	2	
FEM110	ADC125	2	
FEM111	ADC127	2	
FEM112	ADC132	2	
FEM113	ADC126	2	
FEM114	ADC128	2	
FEM115	ADC129	2	
XMIT11			

Figure 21: Crate 1's load

Crate 2		Option	Notes
CTRL02			
FEM16	ADC83	1	
FEM17	ADC74	1	
FEM18	ADC75	1	
FEM20	ADC77	1	
FEM21	ADC78	1	
FEM22	ADC81	1	
FEM23	ADC80	1	
FEM24	ADC24	1	
FEM25	ADC11	1	
FEM26	ADC10	1	
FEM27	ADC9	1	
FEM28	ADC14	1	
FEM29	ADC13	1	
FEM30	ADC12	1	
FEM31	ADC16	1	
XMIT02			

Figure 22: Crate 2's load

Crate 3		Option	Notes
CTRL03			
FEM32	ADC15	1	
FEM34	ADC97	1	
FEM35	ADC96	1	
FEM36	ADC98	1	
FEM37	ADC94	1	
FEM38	ADC95	1	
FEM39	ADC93	1	
FEM40	ADC92	1	
FEM43	ADC88	1	
FEM44	ADC67	1	
FEM45	ADC1	1	
FEM46	ADC2	1	
FEM47	ADC3	1	
FEM48	ADC4	1	
FEM49	ADC5	1	
XMIT03			

Figure 23: Crate 3's load

Crate 4		Option	Notes
CTRL04			
FEM50	ADC6	1	
FEM51	ADC7	1	
FEM52	ADC8	1	
FEM53	ADC33	1	
FEM54	ADC34	1	
FEM55	ADC35	1	
FEM73	ADC36	1	
FEM57	ADC37	1	
FEM58	ADC38	1	
FEM59	ADC39	1	
FEM60	ADC40	1	
FEM61	ADC100	1	
FEM62	ADC99	1	
FEM72	ADC23	1	
FEM64	ADC102	1	
XMIT04			

Figure 24: Crate 4's load

Crate 5		Option	Notes
CTRL5			
FEM67	ADC104	1	
FEM69	ADC106	1	
FEM71	ADC22	1	
FEM74	ADC24	1	
FEM77	ADC112	1	
FEM78	ADC114	1	
FEM121	ADC108	1	
FEM80	ADC48	1	
FEM84	ADC43	1	
FEM85	ADC42	1	
FEM87	ADC44	1	
FEM89	ADC52	1	
FEM90	ADC50	1	
FEM91	ADC49	1	
FEM92	ADC53	1	
XMIT5			

Figure 25: Crate 5's load

Crate 6		Option	Notes
CTRL06			
FEM95	ADC56	1	
FEM123	ADC68	1	
FEM124	ADC69	1	
FEM126	ADC70	1	
FEM127	ADC71	1	
FEM128	ADC29	1	
FEM130	ADC116	1	
FEM131	ADC115	1	
FEM132	ADC117	1	
FEM133	ADC118	1	
FEM135	ADC120	1	
FEM136	ADC121	1	
FEM138	ADC26	1	
FEM139	ADC27	1	
FEM141	ADC30	1	
XMIT06			

Figure 26: Crate 6's load

Crate 7		Option	Notes
CTRL07			
FEM93	ADC54	1	
FEM119	ADC109	1	
FEM142	ADC32	1	
FEM144	ADC17	1	
FEM147	ADC21	1	
FEM79	ADC113	1	
FEM65	ADC103	1	Repaired
FEM68	ADC105	1	Repaired
FEM70	ADC65	1	Repaired
FEM75	ADC110	1	Repaired
FEM76	ADC11	1	Repaired
FEM81	ADC45	1	Repaired
FEM82	ADC47	1	Repaired
FEM83	ADC46	1	Repaired
FEM86	ADC41	1	Repaired
XMIT07			

Figure 27: Crate 7's load

Crate 8		Option	Notes
CTRL08			
FEM88	ADC51	1	Repaired
FEM122	ADC66	1	Repaired
FEM129	ADC73	1	Repaired
FEM134	ADC118	1	Repaired
FEM137	ADC25	1	Repaired
FEM140	ADC28	1	Repaired
FEM143	ADC18	1	Repaired
FEM145	ADC19	1	Repaired
FEM146	ADC20	1	Repaired
FEM66		1	Repaired
FEM19	ADC75	1	DMA Timeout
FEM33	ADC91	1	Data Mismatch (SN test)
FEM56	ADC36	1	DMA Timeout
FEM63	ADC101	1	DMA Timeout
FEM94	ADC55	1	DMA Timeout
XMIT10			

Figure 28: Crate 8's load

Crate 9		Option	Notes
CTRL09			
FEM13	ADC85	1	
FEM14	ADC84	1	
FEM15	ADC82	1	
FEM41	ADC148	2	
FEM42	ADC137	2	
FEM96	ADC140	2	
FEM97	ADC142	2	
FEM98	ADC147	2	
FEM99	ADC141	2	
FEM100	ADC135	2	
FEM101	ADC136	2	
FEM102	ADC144	2	
FEM103	ADC145	2	
FEM104		2	
XMIT09			

Figure 29: Crate 9's load

## VIII. APPENDIX B: BACKPLANE TEST VOLTAGE READINGS

Channel	Voltage before install (V)	Current before install (A)	Voltage before config (V)	Current before config (A)	Voltage after config (V)	Current after config (A)
5V	ok	ok	5.02	6.1	5.02	6.1
12V	ok	ok	12	6	12	12
3.3V	ok	ok	3.3	49	3.29	52
-5V	ok	ok	5.01	3.2	5.01	3.3

Figure 30: Backplane test measurements for crate 1

Channel	Voltage before install (V)	Current before install (A)	Voltage before config (V)	Current before config (A)	Voltage after config (V)	Current after config (A)
5V	5.01	0	5.02	6.5	5.02	6.5
12V	12	0	12	5	12	6
3.3V	3.3	0	3.3	50	3.28	51
-5V	4.9	0	5.01	3.7	5.01	3.7

Figure 31: Backplane test measurements for crate 2

Channel	Voltage before install (V)	Current before install (A)	Voltage before config (V)	Current before config (A)	Voltage after config (V)	Current after config (A)
5V	5.02	6.5	5.02	6.5	5.02	6.5
12V	12	6	12	6	12	12
3.3V	3.3	50	3.3	50	3.3	51
-5V	5.01	3.7	5.01	3.7	5.01	3.7

Figure 32: Backplane test measurements for crate 3

Channel	Voltage before install (V)	Current before install (A)	Voltage before config (V)	Current before config (A)	Voltage after config (V)	Current after config (A)
5V	5.02	6.5	5.02	6.5	5.02	6.5
12V	12	6	12	6	12	6
3.3V	3.3	50	3.3	50	3.3	50
-5V	5.01	3.7	5.01	3.7	5.01	3.7

Figure 33: Backplane test measurements for crate 4

Channel	Voltage before install (V)	Current before install (A)	Voltage before config (V)	Current before config (A)	Voltage after config (V)	Current after config (A)
5V	5.01	6.5	5.01	6.5	5.02	6.5
12V	12	5	12	5	12	6
3.3V	3.3	50	3.3	50	3.3	51
-5V	4.99	3.6	4.99	3.6	5.01	3.7

Figure 34: Backplane test measurements for crate 5

Channel	Voltage before install (V)	Current before install (A)	Voltage before config (V)	Current before config (A)	Voltage after config (V)	Current after config (A)
5V	5.01	6.5	5.01	6.5	5.02	6.5
12V	12	5	12	5	12	6
3.3V	3.3	50	3.3	50	3.3	51
-5V	5	3.6	5	3.6	5.01	3.7

Figure 35: Backplane test measurements for crate 6

Channel	Voltage before install (V)	Current before install (A)	Voltage before config (V)	Current before config (A)	Voltage after config (V)	Current after config (A)
5V	5.02	6.5	5.02	6.5	5.02	6.5
12V	12	5	12	5	12	14
3.3V	3.25	49	3.25	49	3.3	51
-5V	5.01	3.5	5.01	3.5	5.01	3.6

Figure 36: Backplane test measurements for crate 7

Channel	Voltage before install (V)	Current before install (A)	Voltage before config (V)	Current before config (A)	Voltage after config (V)	Current after config (A)
5V	5.01	6.3	5.01	6.3	5.01	6.3
12V	12	5	12	5	12	12
3.3V	3.28	50	3.28	50	3.28	51
-5V	5	3.5	5	3.5	5	3.6

Figure 37: Backplane test measurements for crate 8

Channel	Voltage before install (V)	Current before install (A)	Voltage before config (V)	Current before config (A)	Voltage after config (V)	Current after config (A)
5V	5.01	5.9	5.02	6	5.02	6
12V	12	5	12	12	12	12
3.3V	3.3	50	3.25	50	3.25	51
-5V	5	3.1	5.01	5.9	5.01	3.3

Figure 38: Backplane test measurements for crate 9

## IX. APPENDIX C: FULL ASSEMBLY TESTS

Subrun	linearity	Option 1/2	Option 1/2	Option 1/2
1	Yes	Yes	Yes	Yes
2	Yes	Yes	Yes	Yes
3	Yes	Yes	Yes	Yes
4	Yes	Yes	Yes	Yes

Figure 39: Full assembly subtests for crate 1

Subrun	linearity	Option 1/2	Option 1/2	Option 1/2
1	yes	yes	yes	yes
2	yes	yes	yes	yes
3	yes	yes	yes	yes
4	yes	yes	yes	yes
5	yes	yes	yes	yes

Figure 40: Full assembly subtests for crate 2

Subrun	linearity	Option 1/2	Option 1/2	Option 1/2
1	yes	yes	yes	yes
2	yes	yes	yes	yes
3	yes	yes	yes	yes
4	yes	yes	yes	yes
5	yes	yes	yes	yes

Figure 41: Full assembly subtests for crate 3

Subrun	linearity	Option 1/2	Option 1/2	Option 1/2
1	yes	yes	yes	yes
2	yes	yes	yes	yes
3	yes	yes	yes	yes
4	yes	yes	yes	yes
5	yes	yes	yes	yes

Figure 42: Full assembly subtests for crate 4

Subrun	linearity	Option 1/2	Option 1/2	Option 1/2
1	yes	yes	yes	yes
2	yes	yes	yes	yes
3	yes	yes	yes	yes
4	yes	yes	yes	yes
5	yes	yes	yes	yes

Figure 43: Full assembly subtests for crate 5

Subrun	linearity	Option 1/2	Option 1/2	Option 1/2
1	yes	yes	yes	yes
2	yes	yes	yes	yes
3	yes	yes	yes	yes
4	yes	yes	yes	yes
5	yes	yes	yes	yes

Figure 44: Full assembly subtests for crate 6

Subrun	linearity ok?	Option 1/2	Option 1/2 RP	Option 1/2
1	yes	yes	yes	yes
2	yes	yes	yes	yes
3	yes	yes	yes	yes
4	yes	yes	yes	yes
5	yes	yes	yes	yes

Figure 45: Full assembly subtests for crate 7

Subrun	linearity ok?	Option 1/2 baselines ok?	Option 1/2 RMS ok?	Option 1/2
1	Yes	Yes	Yes	Yes
2	Yes	Yes	Yes	Yes
3	Yes	Yes	Yes	Yes
4	Yes	Yes	Yes	Yes
5	Yes	Yes	Yes	Yes

Figure 46: Full assembly subtests for crate 8

Subrun	linearity ok?	Option 1/2	Option 1/2	Option 1/2
1	Yes	Yes	Yes	Yes
2	Yes	Yes	Yes	Yes
3	Yes	Yes	Yes	Yes
4	Yes	Yes	Yes	Yes
5	Yes	Yes	Yes	Yes

Figure 47: Full assembly subtests for crate 9