

TPC Electronics and Readout Prototype II Test Results

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This document reports the complete results from the joint BNL/Nevis Prototype II tests performed in August 2012.

1 Setup Description

A prototype test stand was set up at Nevis Laboratories to replicate a slice of the entire MicroBooNE electronics readout chain. The electronic signal from the TPC wires are simulated using a modified (9U) trigger board, a function generator (AFG3252), and a “Toy TPC” capacitor circuit. The signals are read out in “calibration” mode, where the readout software drives the signal generation (via trigger board sitting in the TPC readout crate which signals the AFG3252), and then reads the data through either XMIT or crate controller (slow readout).

A pulser is used to provide a higher-amplitude trigger to the function generator than what is actually provided by the trigger board. The function generator (configured using AFG3252) fires when it receives the trigger from the pulser. The “Toy TPC” circuit uses a capacitor to induce a unipolar or bipolar pulse, depending on function generator frequency (the default setting of 10 kHz induces a unipolar pulse), when an input voltage differential is produced by the AFG3252. A bipolar pulse is always generated by the function generator. The way the function generator frequency determines whether the pulse is unipolar or bipolar is based on the observation window of the electronics downstream. If the window is too short relative to the pulse frequency (low frequency), then the electronics will only observe the negative voltage portion of the pulse and the signal will be a unipolar pulse. If the window is long relative to the pulse frequency (high frequency), then the electronics will observe both the negative and positive voltage portion of the pulse and the signal will be a bipolar pulse.

The pulses are inverted pulses and have a frequency of 10 kHz (100 μ s period) with a duty cycle of 60% and rise/fall time of 40 ns and an adjustable voltage height from 0 mV to several V. A typical charged particle would induce an electronic pulse that is roughly 600 mV in height. Figure 1 shows the input voltage. The pulses act as delta functions and allow the shaping of the ASICs and the effect of the electronic readout to be clearly seen.

The pulses are then sent to a miniature faraday box (designed for the electronics and readout tests and not the same as the faraday box in the actual MiniBooNE design), which simulates the MicroBooNE cryostat chamber. In the miniature faraday box are 48 ASIC chips (16 channels each). The signals are amplified and shaped by the ASICs and passed on to the intermediate amplifiers located directly above the ASICs. The further amplified signals then leave the miniature faraday box through the service boards located above the intermediate amplifiers. The signals are finally sent to twelve FEM boards, where the data can be digitized at 2 MHz and read out through the crate (slow readout) or the XMIT board controller (fast readout). The data is sent via optical cables and PCIe boards to a nearby computer for collection and analysis. A photo of the entire prototype test stand (minus the readout computer) can be seen in Figure 2. Figure 3 shows the 12 FEM boards along with the XMIT, trigger, and controller board in the crate.

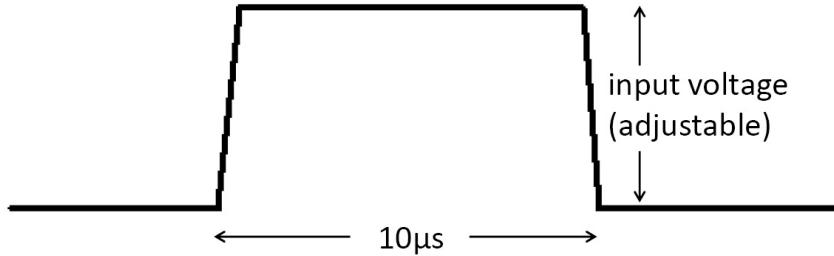


Figure 1: A representative shape of the input pulse from AFG3252. Note that the actual pulse is inverted.

2 Tests Performed

The following tests were performed:

- Baseline ADC measurements.
- Linearity test from baseline to ADC saturation.
- ASIC channel-to-channel crosstalk within each ASIC chip.
- ASIC chip-to-chip crosstalk within each ADC motherboard with default gain and peaking time.

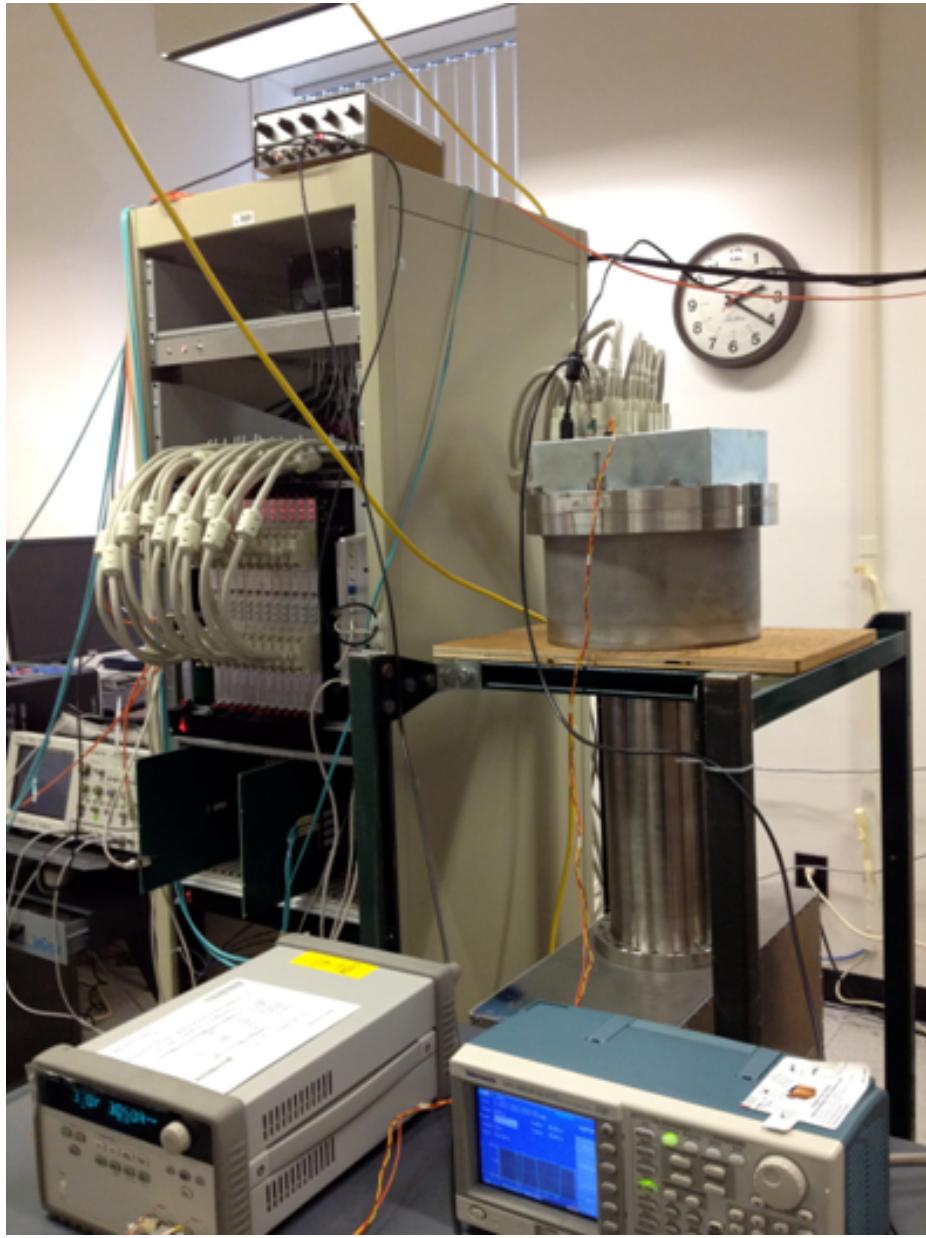


Figure 2: Photo of the entire prototype test stand.

3 Output Signals

Figure 4 shows sample ADC baselines for induction and collection wires for a single channel using XMIT readout. Figure 5 shows sample ADC peaks for



Figure 3: Photo of the FEM crate with the 12 FEM boards and XMIT board.

induction and collection wires for a single channel with 600 mV input pulse voltage using XMIT readout. The default gain setting of 4.7 mV/fC and peaking time of 2 μ s are used. 1000 pulses are used.

Figure 6 shows the mean and RMS for ADC voltage and time for all channels in FEM1 during baseline (no input test pulse) using XMIT readout. Figure 7 shows the mean and RMS for ADC voltage and time for all channels in FEM1 with 600 mV input test pulse using XMIT readout.

Figures 8 and 9 shows the max ADC distribution for 1000 events for 8 induction wire channels and collection wire channels. The input pulse voltage is 600 mV. The figures show that the max ADC clusters around specific ADC values, creating 4 separate distributions of max ADC values per channel.

Figures 10 to 12 shows the baseline ADC voltage for all channels of all FEMs

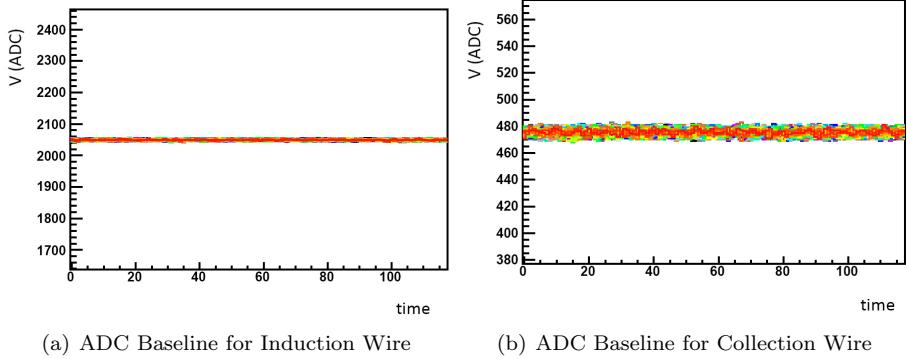


Figure 4: Sample ADC baselines for induction and collection wires for a single channel (XMIT readout).

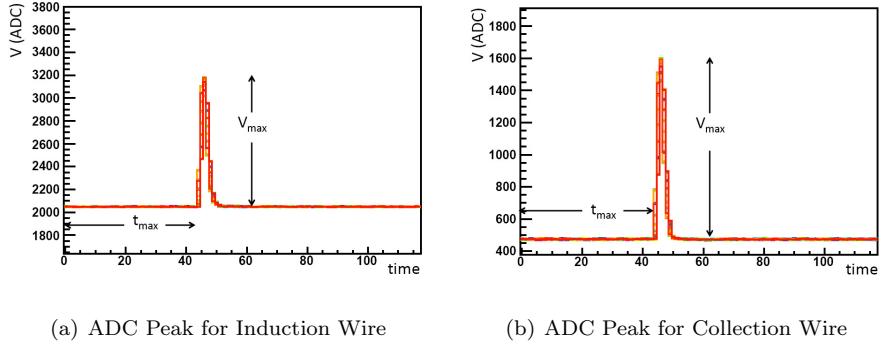


Figure 5: Sample ADC peaks for induction and collection wires for a single channel with 600 mV input pulse voltage (XMIT readout). Note that the bipolar shape of induction wire pulses is a consequence of field response. Here, the electronics response is being tested so a unipolar test pulse is satisfactory for the tests.

using XMIT readout. Note that channels 0-31 is for the induction wires and have the higher baselines and channels 32-63 is for the collection wires and have the lower baselines.

4 Linearity Tests

The input pulse voltage and the resulting ADC values should follow a linear relationship until ADC saturation. To test this using both the slow and XMIT readout, the input pulse voltage was increased from 0 mV to saturation voltage

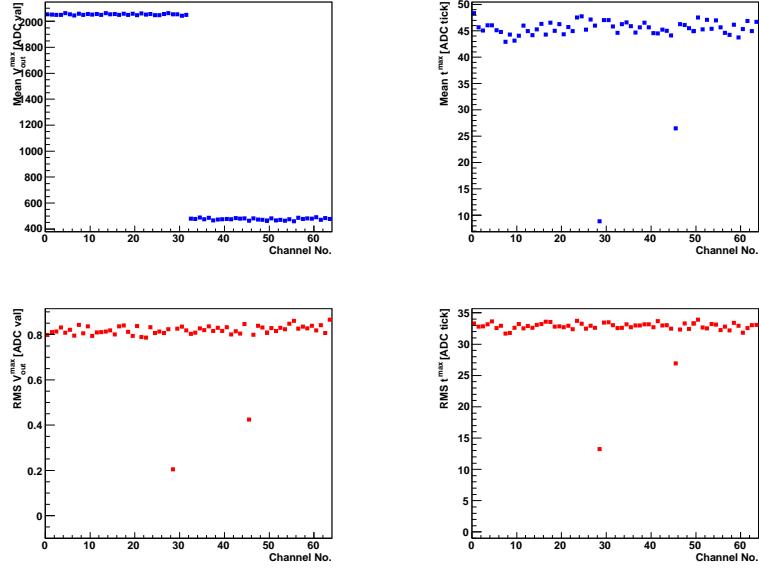


Figure 6: The mean and RMS for ADC voltage and time for all channels from FEM1 at baseline (XMIT readout).

(about 850 mV for all channels and FEMs) in increments of 50 mV. Figures 15 to 17 shows the linear relationship between input pulse voltage and resulting ADC voltage for FEM1-FEM12 until ADC saturation (850 mV) using slow controller readout. Each figure shows all 64 channels of one FEM overlayed.

Figures 13 and 14 show the slope and intercept distributions for linearity between input pulse voltage (in V) and ADC values for all induction and collection wire channels of all FEM. The Gaussian fits for all four distributions are also included. For the Gaussian fits of the linearity distributions containing the induction wire channels, the mean is 1927 ADC/V with a standard deviation of 14 ADC/V and the intercept is 2047 ADC/V with a standard deviation of 5 ADC/V. For the Gaussian fits of the linearity distributions containing the collection wire channels, the mean is 1926 ADC/V with a standard deviation of 16 ADC/V and the intercept is 473 ADC/V with a standard deviation of 7 ADC/V.

From the linearity tests, all the channels of all the FEMs deviate from the previous linearity and saturates at around 900 mV to 950 mV input voltage.

The fractional residual percentage, defined as $\frac{\text{Data} - \text{Fit}}{\text{Fit}} \times 100\%$ where *Fit* is the linear fit for each channel of every FEM, can be seen in figs. 18 to 20. The

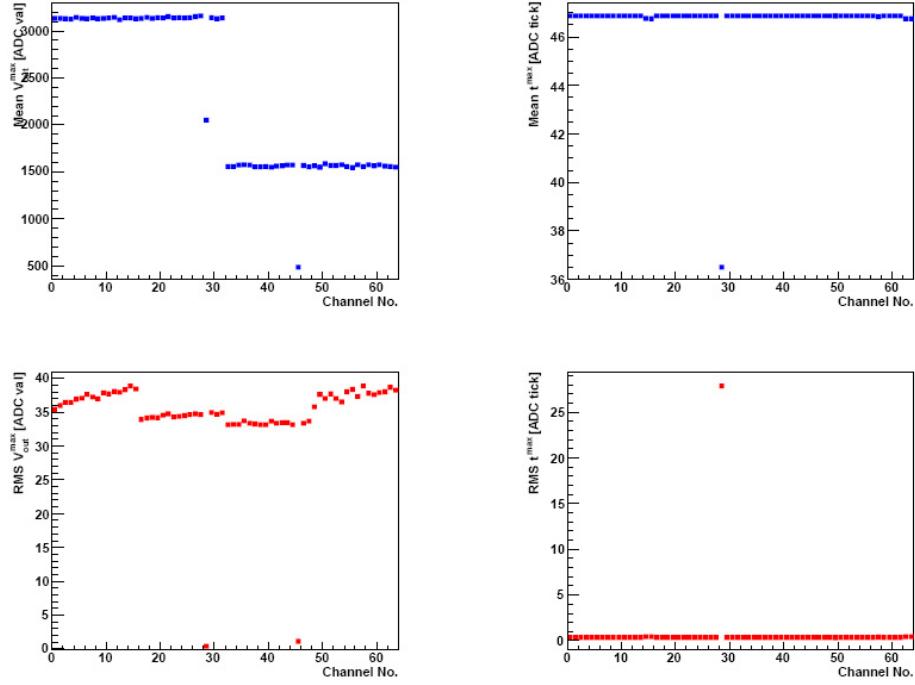


Figure 7: The mean and RMS for ADC voltage and time for all channels from FEM1 with 600 mV input test pulse (XMIT readout).

fractional residual percentage shows the deviations from the fitted linear relationship for each channel of every FEM. The figures show that for all channels of all FEM, the fractional residual percentage is well within $+1.5\%$ and -1.0% , except for channel 18 of FEM3, which has a very large and abnormal linear fit slope relative to all the other channels.

Figures 21 to 32 shows two-dimensional plots of V_{max} , RMS of V_{max} , t_{max} , and RMS of t_{max} as a function of both input pulse voltage (in V) and channel number for FEM1-FEM12.

The linearity tests show that the linearity between input voltage and ADC values is observed for almost all the channels (with very few exceptions) of all the FEMs to a high degree with very little deviations between input voltages of 50 mV to 850 mV. The slope and intercept of the linearity is also very consistent among the different channels of the FEMs for both induction and collection wires.

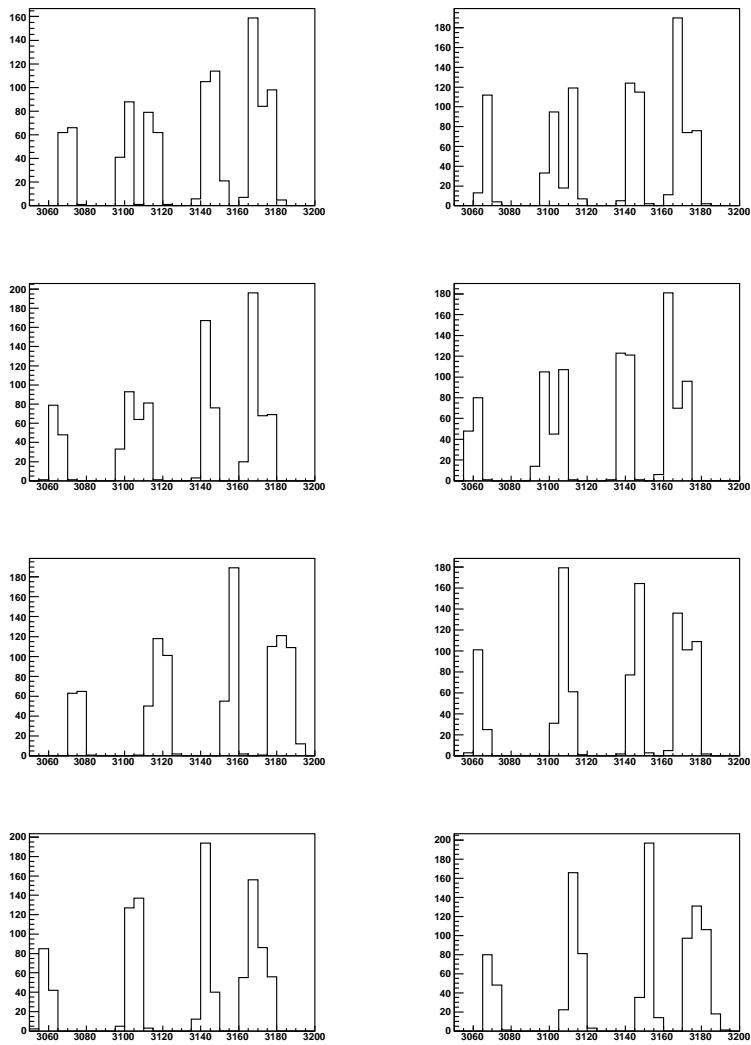


Figure 8: Max ADC distribution for 1000 events for 8 induction wire channels (0-7) in FEM1. The input pulse voltage is 600 mV.

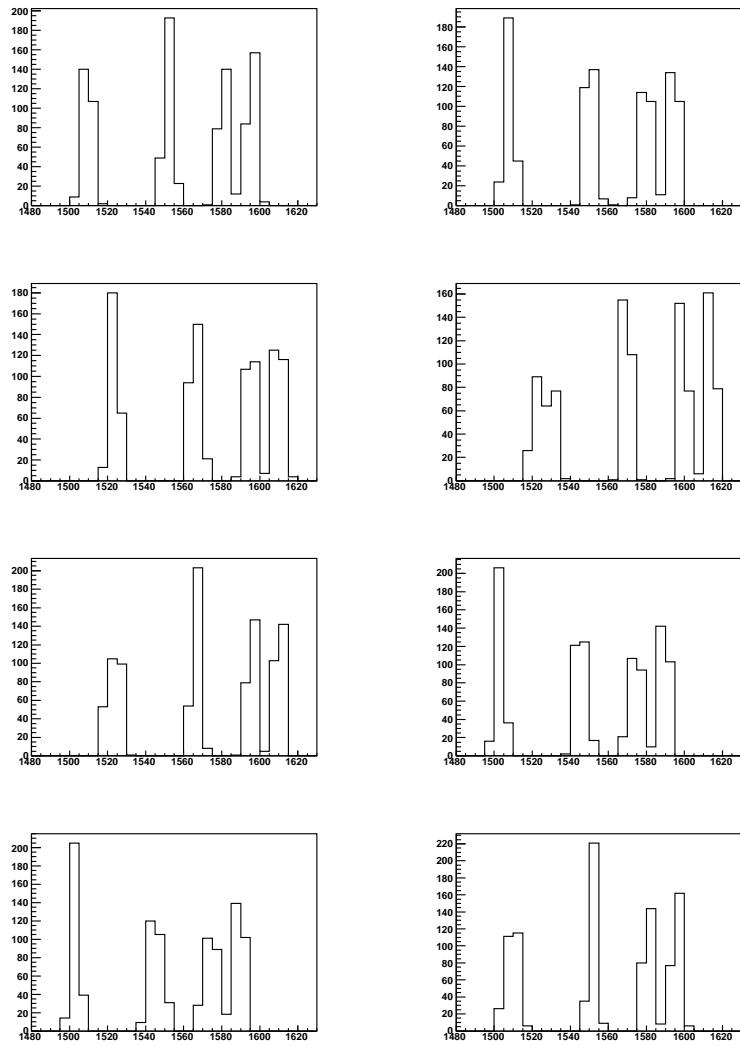


Figure 9: Max ADC distribution for 1000 events for 8 collection wire channels (32-39) in FEM1. The input pulse voltage is 600 mV.

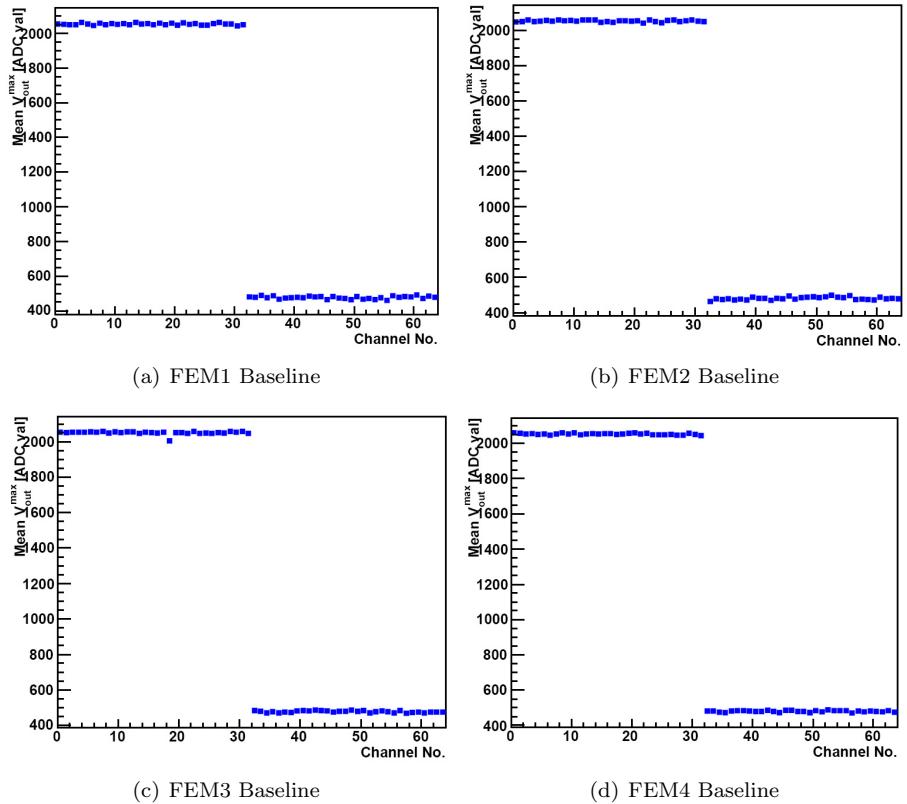


Figure 10: Baseline values of all channels for FEM1-4 (XMIT readout).

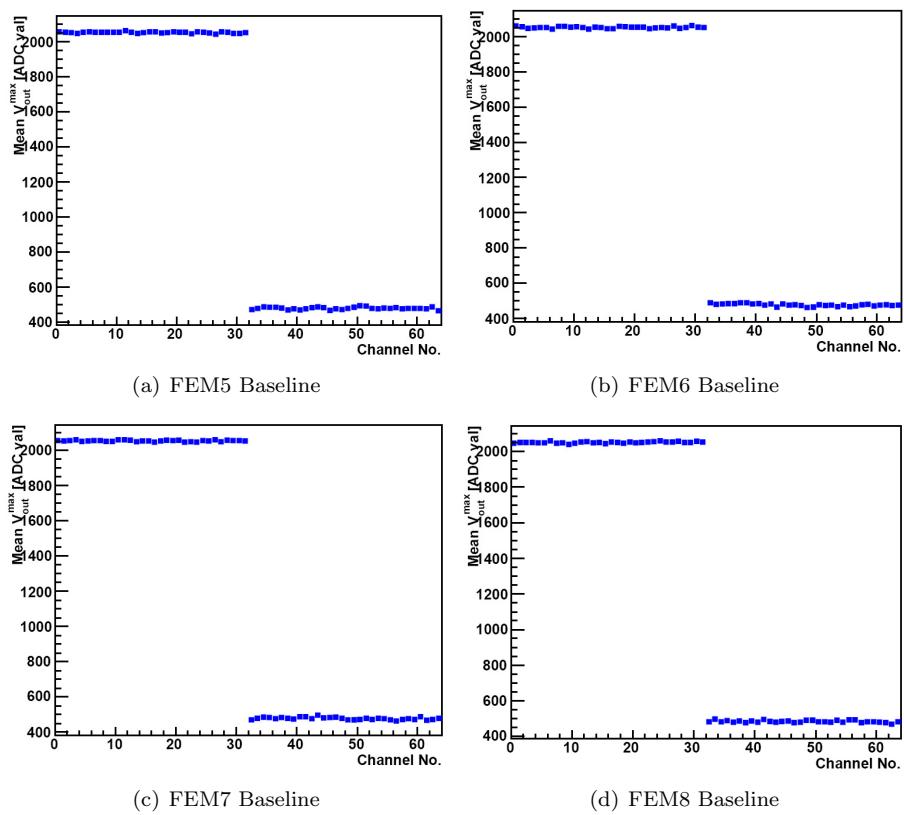


Figure 11: Baseline values of all channels for FEM5-8 (XMIT readout).

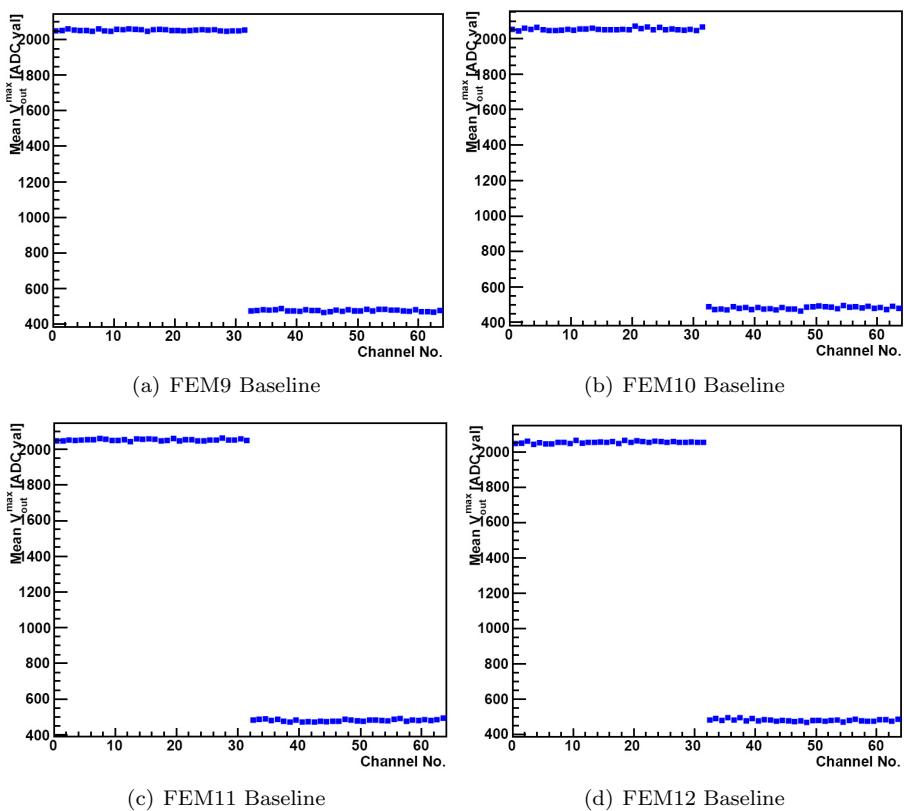


Figure 12: Baseline values of all channels for FEM9-12 (XMIT readout).

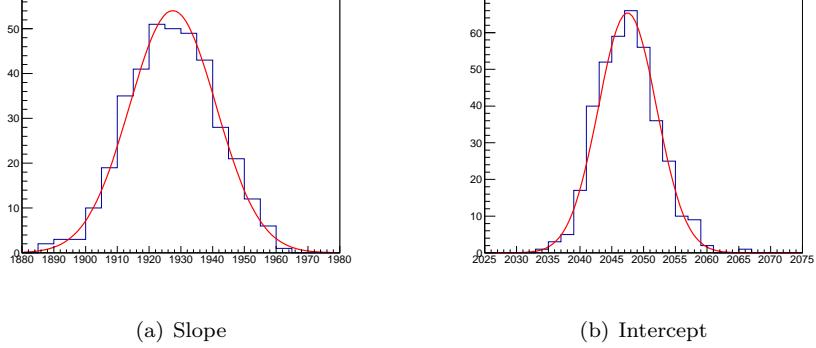


Figure 13: The blue histograms show the distribution of the slope (left) and intercept (right) for the linearity between input pulse voltage (in V) and ADC values for all induction wire channels of all FEM. The red lines show the Gaussian fits to the distributions.

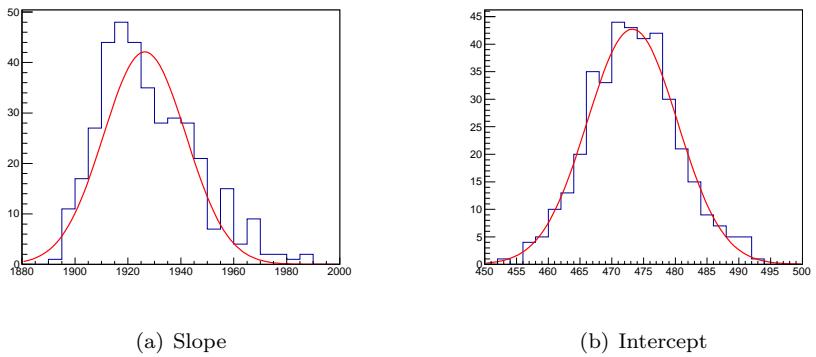


Figure 14: The blue histograms show the distribution of the slope (left) and intercept (right) for the linearity between input pulse voltage (in V) and ADC values for all collection wire channels of all FEM. The red lines show the Gaussian fits to the distributions.

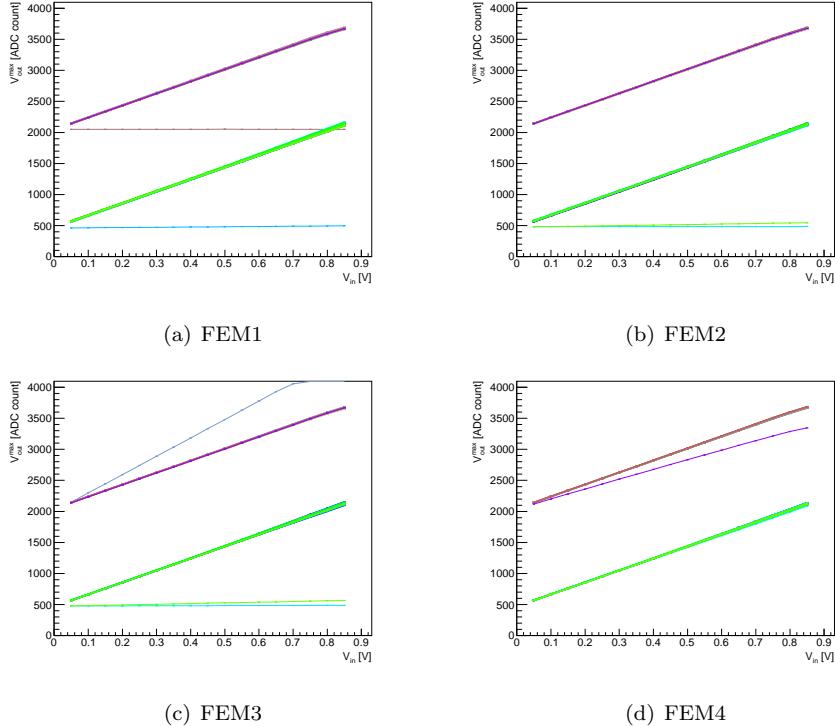


Figure 15: The linear relationship between input pulse voltage (using AFG3252) and resulting ADC voltage for all 64 channels (0-63) in FEM1 (top left), FEM2 (top right), FEM3 (bottom left), FEM4 (bottom right). For FEM1, the horizontal lines represent the bad ASIC channels 28,45. For FEM2, the horizontal lines represent the bad ASIC channels 47,63. For FEM3, the horizontal lines represent the bad ASIC channels 47,63.

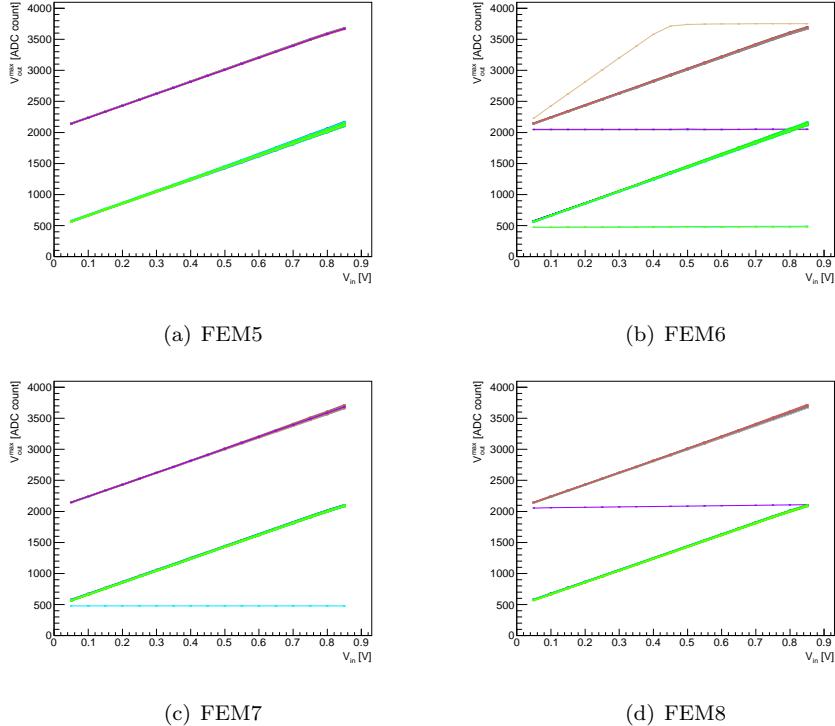


Figure 16: The linear relationship between input pulse voltage (using AFG3252) and resulting ADC voltage for all 64 channels (0-63) in FEM5 (top left), FEM6 (top right), FEM7 (bottom left), FEM8 (bottom right). For FEM6, the horizontal lines represent the bad ASIC channels 15,23,31,47,63. For FEM7, the horizontal line represents the bad ASIC channel 47. For FEM8, the horizontal line represents the bad ASIC channel 31.

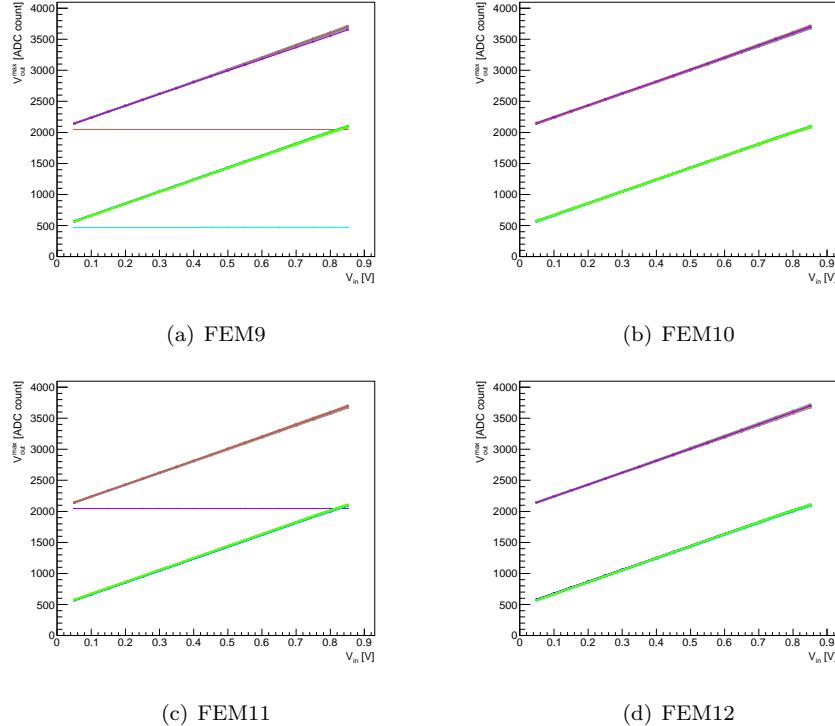


Figure 17: The linear relationship between input pulse voltage (using AFG3252) and resulting ADC voltage for all 64 channels (0-63) in FEM9 (top left), FEM10 (top right), FEM11 (bottom left), FEM12 (bottom right). For FEM9, the horizontal lines represent the bad ASIC channels 30,47. For FEM11, the horizontal line represents the bad ASIC channel 31.

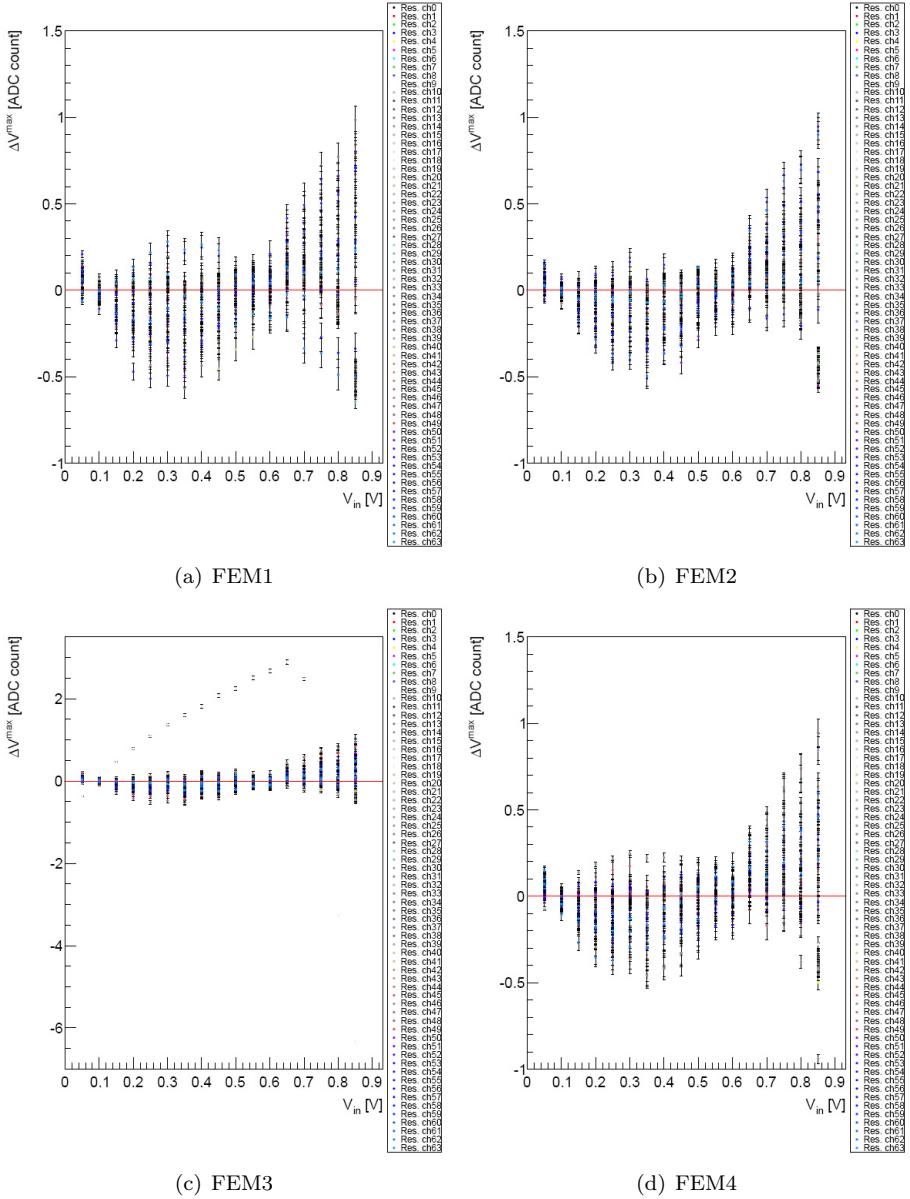


Figure 18: The fractional residual percentage ($\frac{\text{Data}-\text{Fit}}{\text{Fit}} \times 100\%$) from the linear relationship for all 64 channels in FEM1 (top left), FEM2 (top right), FEM3 (bottom left), FEM4 (bottom right) as a function of input pulse voltage.

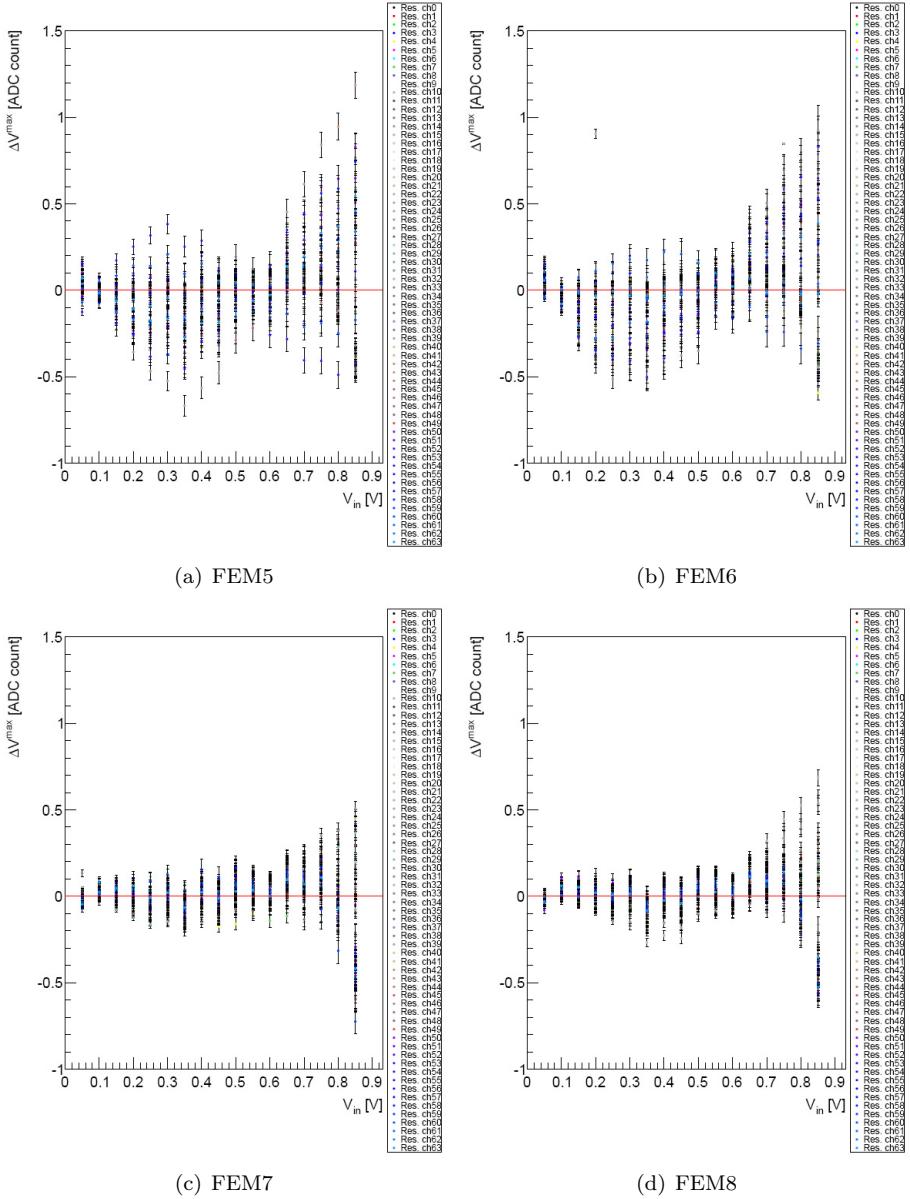


Figure 19: The fractional residual percentage ($\frac{\text{Data} - \text{Fit}}{\text{Fit}} \times 100\%$) from the linear relationship for all 64 channels in FEM5 (top left), FEM6 (top right), FEM7 (bottom left), FEM8 (bottom right) as a function of input pulse voltage.

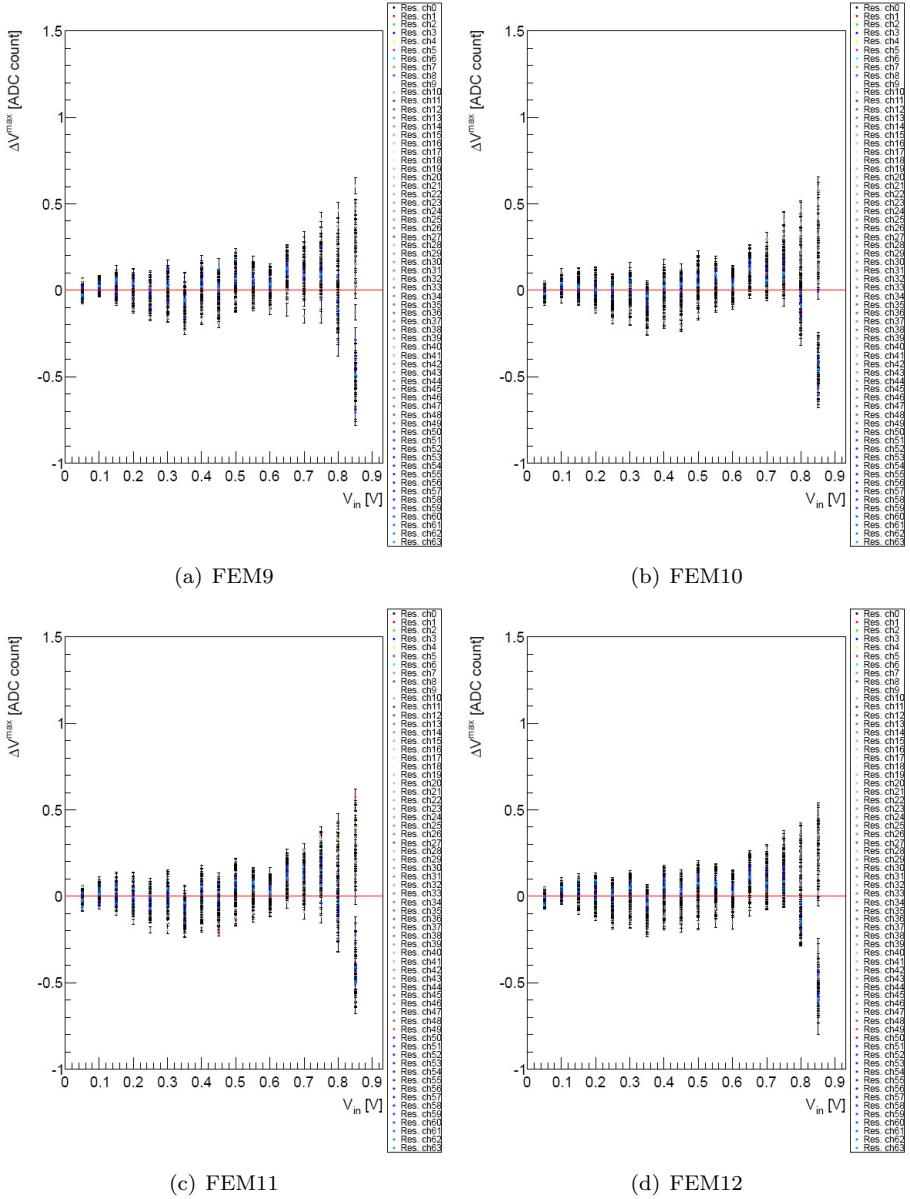


Figure 20: The fractional residual percentage ($\frac{\text{Data} - \text{Fit}}{\text{Fit}} \times 100\%$) from the linear relationship for all 64 channels in FEM9 (top left), FEM10 (top right), FEM11 (bottom left), FEM12 (bottom right) as a function of input pulse voltage.

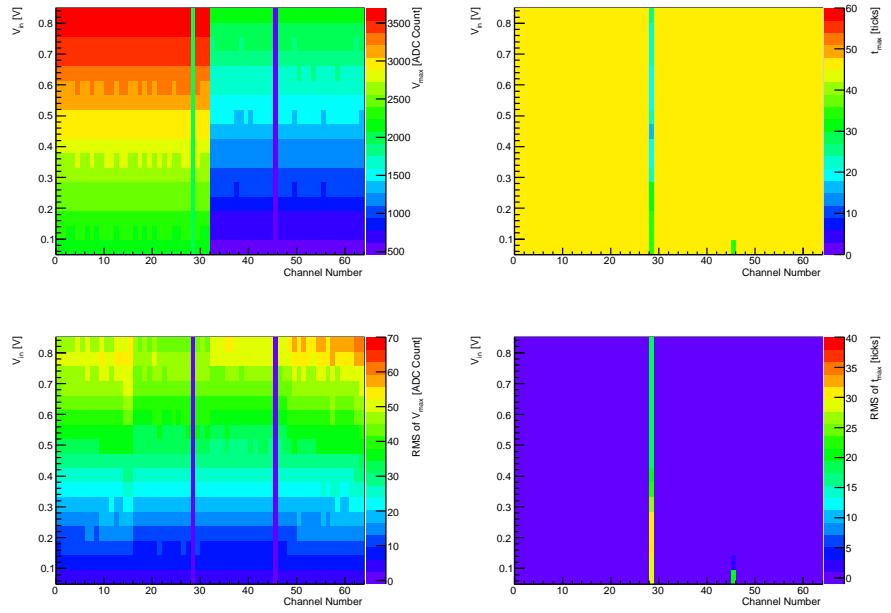


Figure 21: Two-dimensional plots of V_{max} , RMS of V_{max} , t_{max} , and RMS of t_{max} as a function of both input pulse voltage (in V) and channel number for FEM1. The bad ASIC channels (28,45) can be easily identified by their significant different values relative to their neighboring normal ASIC channels.

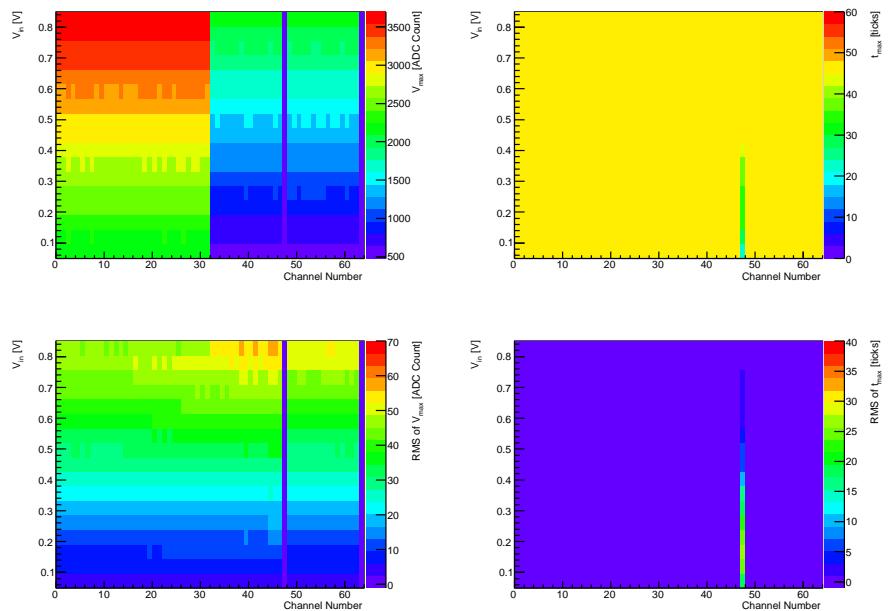


Figure 22: Two-dimensional plots of V_{max} , RMS of V_{max} , t_{max} , and RMS of t_{max} as a function of both input pulse voltage (in V) and channel number for FEM2. The bad ASIC channels (47,63) can be easily identified by their significant different values relative to their neighboring normal ASIC channels.

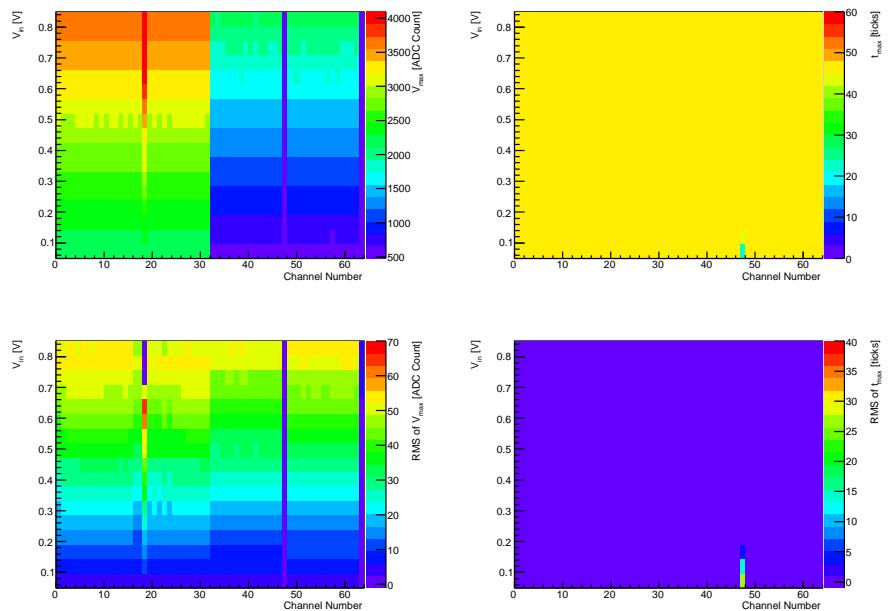


Figure 23: Two-dimensional plots of V_{max} , RMS of V_{max} , t_{max} , and RMS of t_{max} as a function of both input pulse voltage (in V) and channel number for FEM3. The bad ASIC channels (47,63) can be easily identified by their significant different values relative to their neighboring normal ASIC channels.

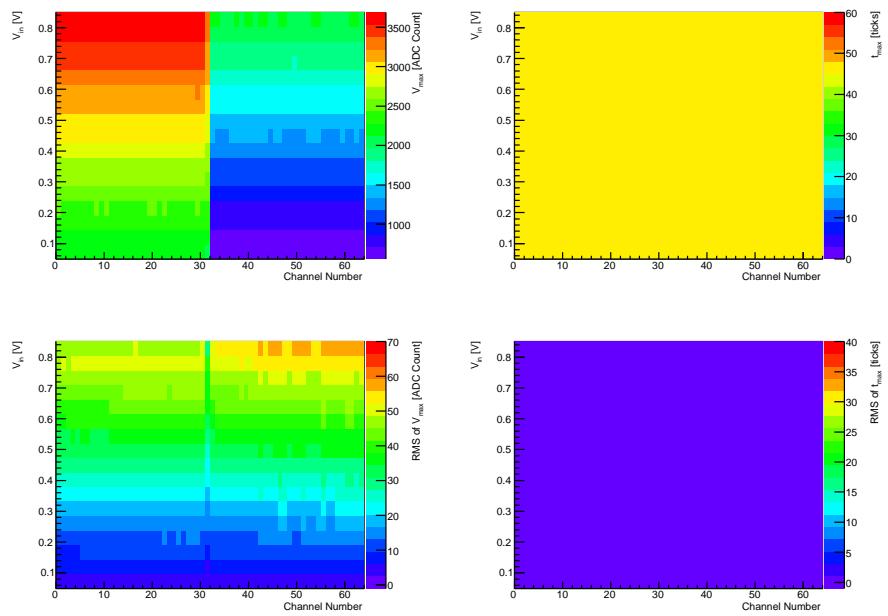


Figure 24: Two-dimensional plots of V_{max} , RMS of V_{max} , t_{max} , and RMS of t_{max} as a function of both input pulse voltage (in V) and channel number for FEM4.

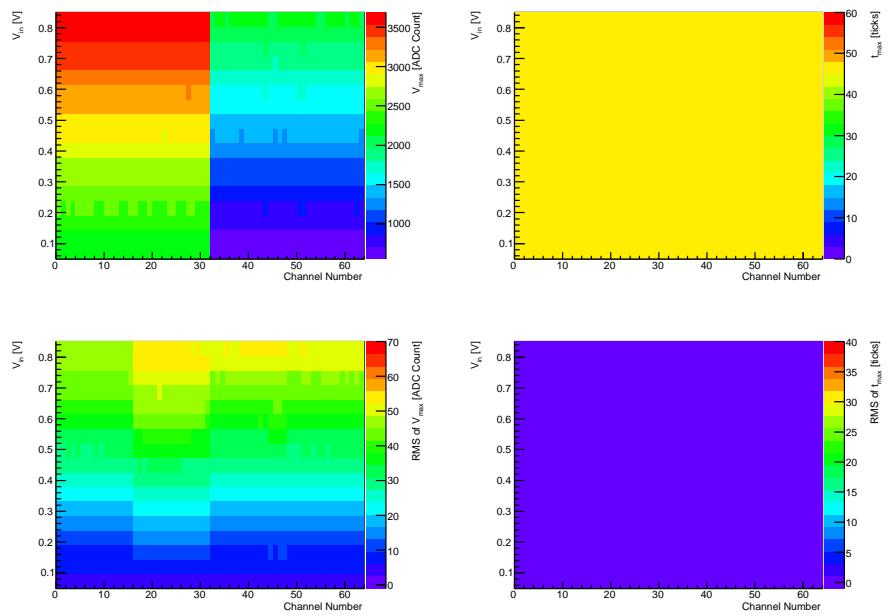


Figure 25: Two-dimensional plots of V_{max} , RMS of V_{max} , t_{max} , and RMS of t_{max} as a function of both input pulse voltage (in V) and channel number for FEM5.

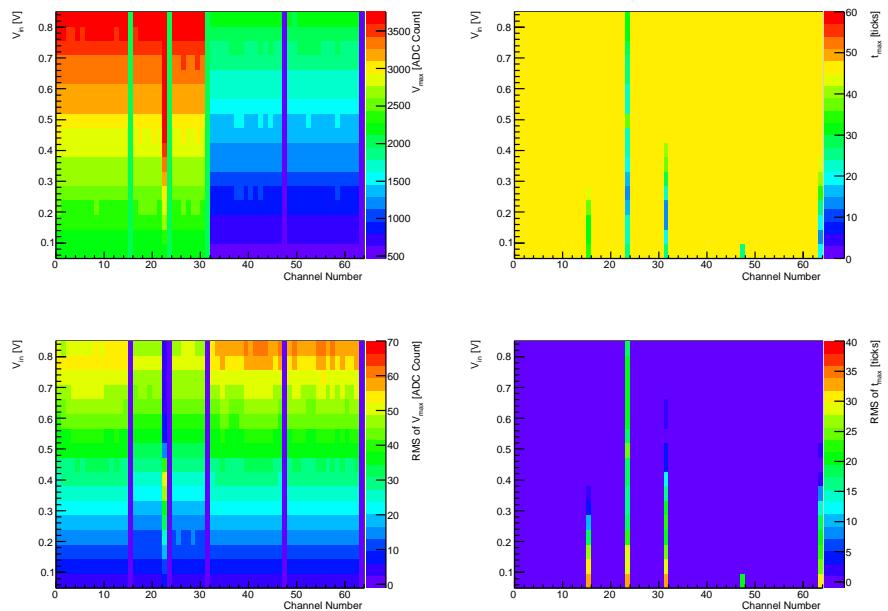


Figure 26: Two-dimensional plots of V_{max} , RMS of V_{max} , t_{max} , and RMS of t_{max} as a function of both input pulse voltage (in V) and channel number for FEM6. The bad ASIC channels (15,23,31,47,63) can be easily identified by their significant different values relative to their neighboring normal ASIC channels.

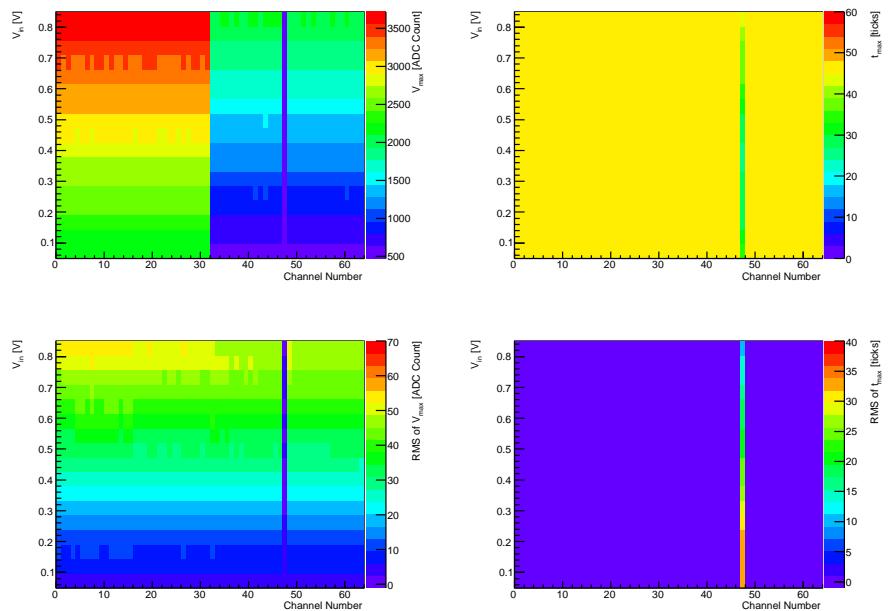


Figure 27: Two-dimensional plots of V_{max} , RMS of V_{max} , t_{max} , and RMS of t_{max} as a function of both input pulse voltage (in V) and channel number for FEM7. The bad ASIC channel (47) can be easily identified by their significant different values relative to their neighboring normal ASIC channels.

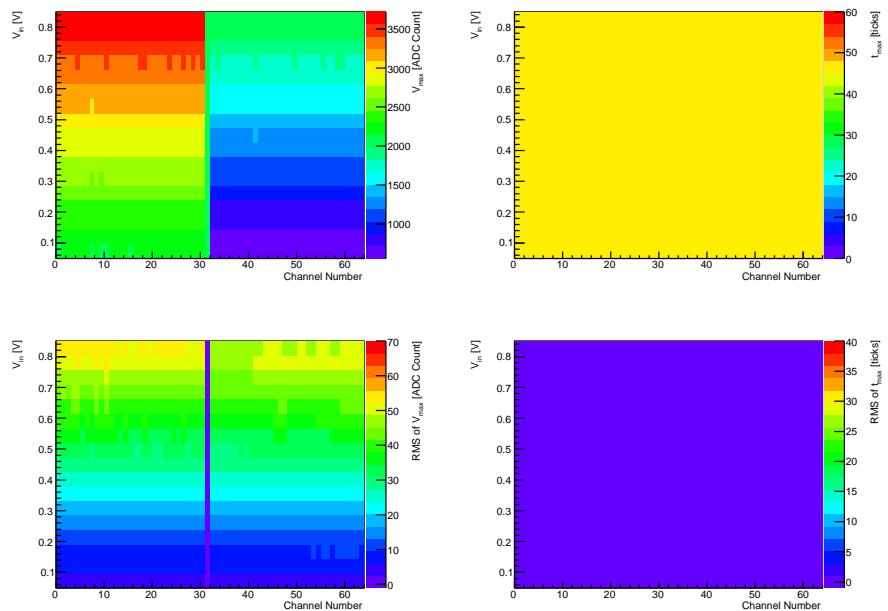


Figure 28: Two-dimensional plots of V_{max} , RMS of V_{max} , t_{max} , and RMS of t_{max} as a function of both input pulse voltage (in V) and channel number for FEM8. The bad ASIC channel (31) can be easily identified by their significant different values relative to their neighboring normal ASIC channels.

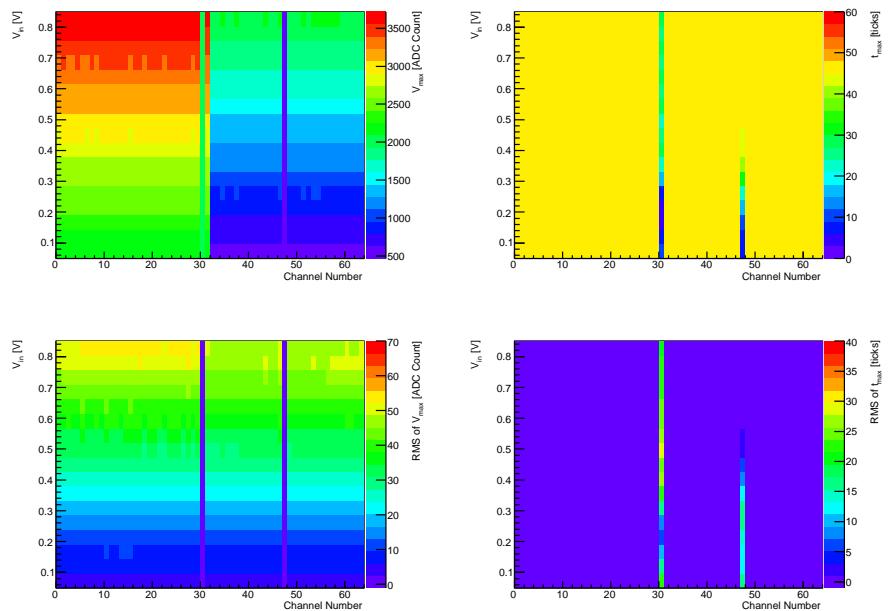


Figure 29: Two-dimensional plots of V_{max} , RMS of V_{max} , t_{max} , and RMS of t_{max} as a function of both input pulse voltage (in V) and channel number for FEM9. The bad ASIC channels (30,47) can be easily identified by their significant different values relative to their neighboring normal ASIC channels.

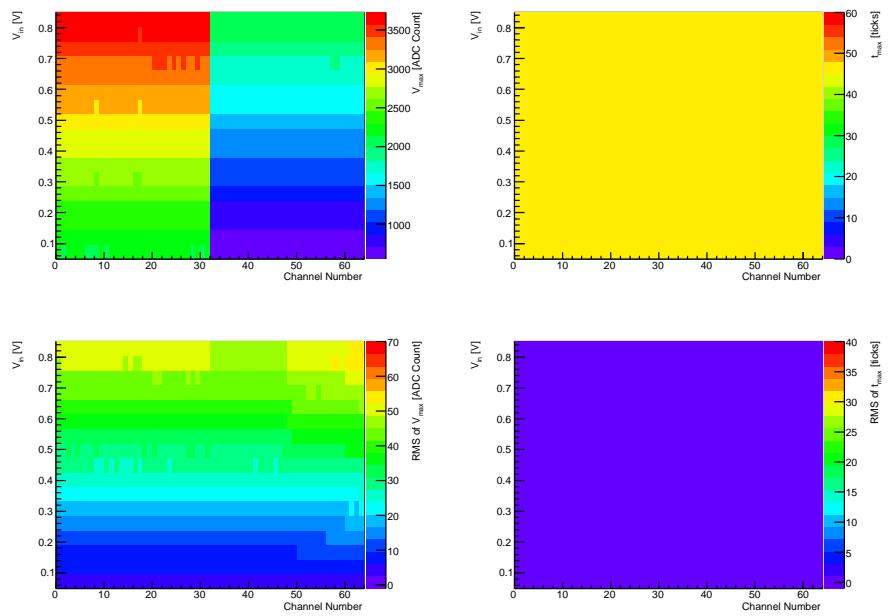


Figure 30: Two-dimensional plots of V_{max} , RMS of V_{max} , t_{max} , and RMS of t_{max} as a function of both input pulse voltage (in V) and channel number for FEM10.

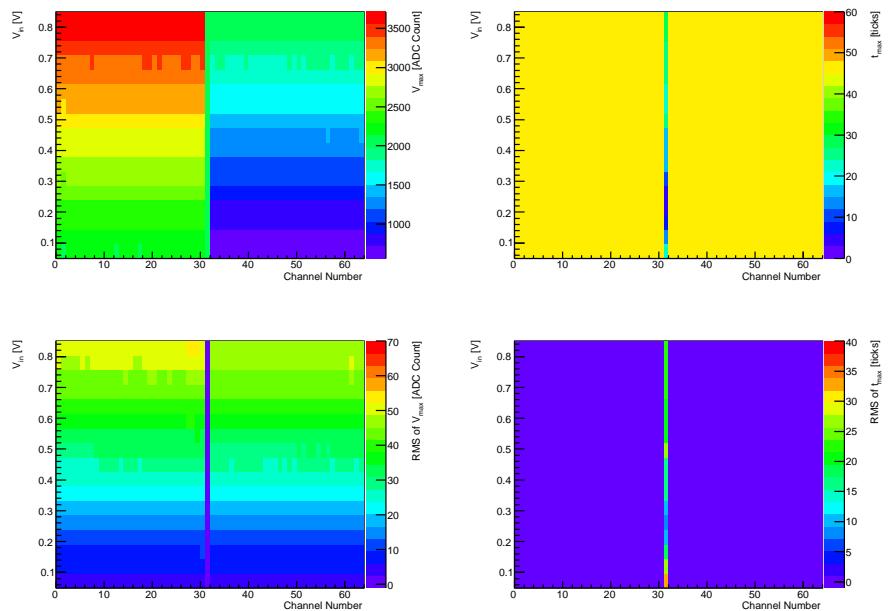


Figure 31: Two-dimensional plots of V_{max} , RMS of V_{max} , t_{max} , and RMS of t_{max} as a function of both input pulse voltage (in V) and channel number for FEM11. The bad ASIC channel (31) can be easily identified by their significant different values relative to their neighboring normal ASIC channels.

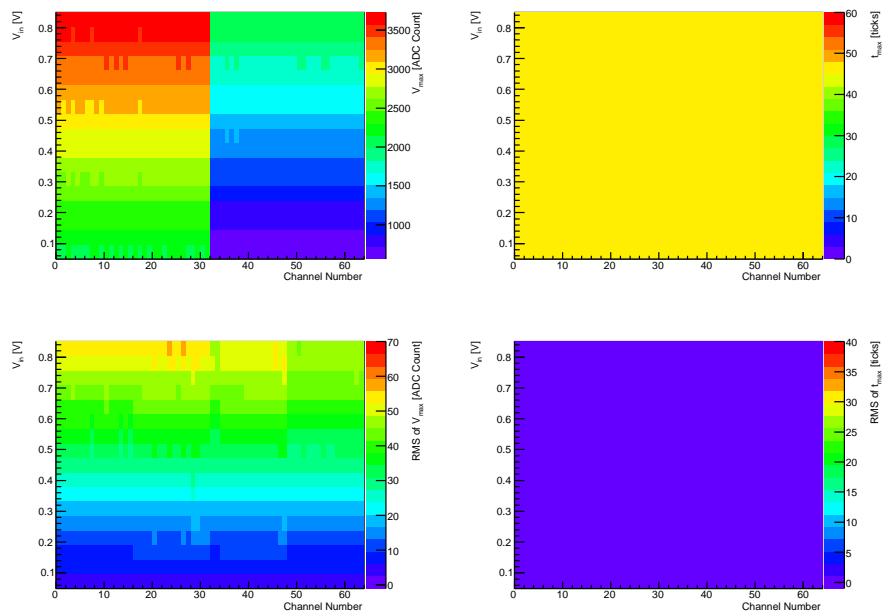


Figure 32: Two-dimensional plots of V_{max} , RMS of V_{max} , t_{max} , and RMS of t_{max} as a function of both input pulse voltage (in V) and channel number for FEM12.

5 ASIC Channel-to-Channel Crosstalk

Based on the description in section 10, to test the channel-to-channel crosstalk, a 600 mV test pulse is sent to each ASIC chip, which has one channel unmasked with all other 15 channels masked. The bad ASIC channels in section 11 are always masked. Figures 35 and 36 show the channel-to-channel crosstalk for ASIC chip 1 with channel 1 unmasked (corresponding to FEM7 channels 32-47 with channel 32 unmasked). Figure 33 and 34 show the channel-to-channel crosstalk for ASIC chip 2 with channel 1 unmasked (corresponding to FEM7 channels 16-31 with channel 16 unmasked).

For a induction wire channel that is pulsed (600 mV test pulse), the channel-to-channel crosstalk on another induction wire channel is a tiny positive ADC valued peak with a height about 1.2% the height of the original pulsed induction wire channel (14 ADC values above baseline for crosstalk peak compared to 1200 ADC values above baseline for pulsed peak). The crosstalk channel peaks are consistent among all 15 of the other un-pulsed induction wire channels of the ASIC.

For a collection wire channel that is pulsed (600 mV test pulse), the channel-to-channel crosstalk on another collection wire channel is a tiny negative ADC peak followed by a tiny positive ADC valued peak with both peaks roughly the same deviation from baseline. Each of the peaks has a height about 1.2% the height of the original pulsed collection wire channel (14 ADC values from baseline for crosstalk peak compared to 1200 ADC values above baseline for pulsed peak). The crosstalk channel peaks are consistent among all 15 of the other un-pulsed collection wire channels of the ASIC.

6 ASIC Chip-to-Chip Crosstalk

Based on the description in section 10, to test the chip-to-chip crosstalk, a 600 mV test pulse is sent to each ASIC motherboard, which has one ASIC chip unmasked with all other 11 ASIC chips masked. The bad ASIC channels in section 11 are always masked. Figure 37 shows the chip-to-chip crosstalk in ASIC chip 2 (induction wire ASIC) for ASIC chip 1 (collection wire ASIC) unmasked (corresponding to FEM7 channels 32-47). Figure 38 shows the chip-to-chip crosstalk in ASIC chip 3 (collection wire ASIC) for ASIC chip 1 (collection wire ASIC) unmasked (corresponding to FEM7 channels 32-47). Figure 39 shows the chip-to-chip crosstalk in ASIC chip 1 (collection wire ASIC) for ASIC chip 2 (induction wire ASIC) unmasked (corresponding to FEM7 channels 16-31). Figure 40 shows the chip-to-chip crosstalk in ASIC chip 4 (induction wire ASIC) for ASIC chip 2 (induction wire ASIC) unmasked (corresponding to FEM7 channels 16-31).

For an collection wire ASIC that is pulsed (600 mV test pulse), the chip-to-chip crosstalk on another induction wire ASIC is a negative ADC peak followed by a tiny positive ADC valued peak with both peaks roughly the same deviation from baseline. Each of the induction wire ASIC channel peaks has a height about

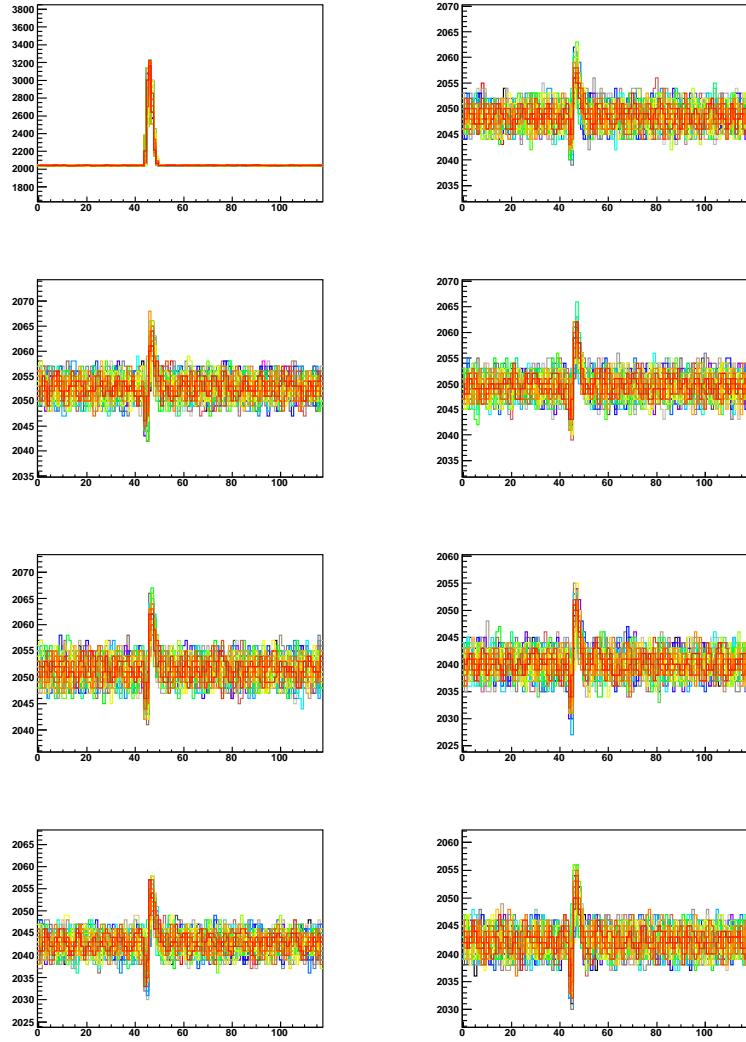


Figure 33: Channel-to-channel crosstalk of channels 1-8 for ASIC chip 2 with channel 1 unmasked (corresponding to FEM7 channels 16-23 with channel 16 unmasked). A 600 mV test pulse is sent to each ASIC chip. Note this is for induction wire ADC baseline.

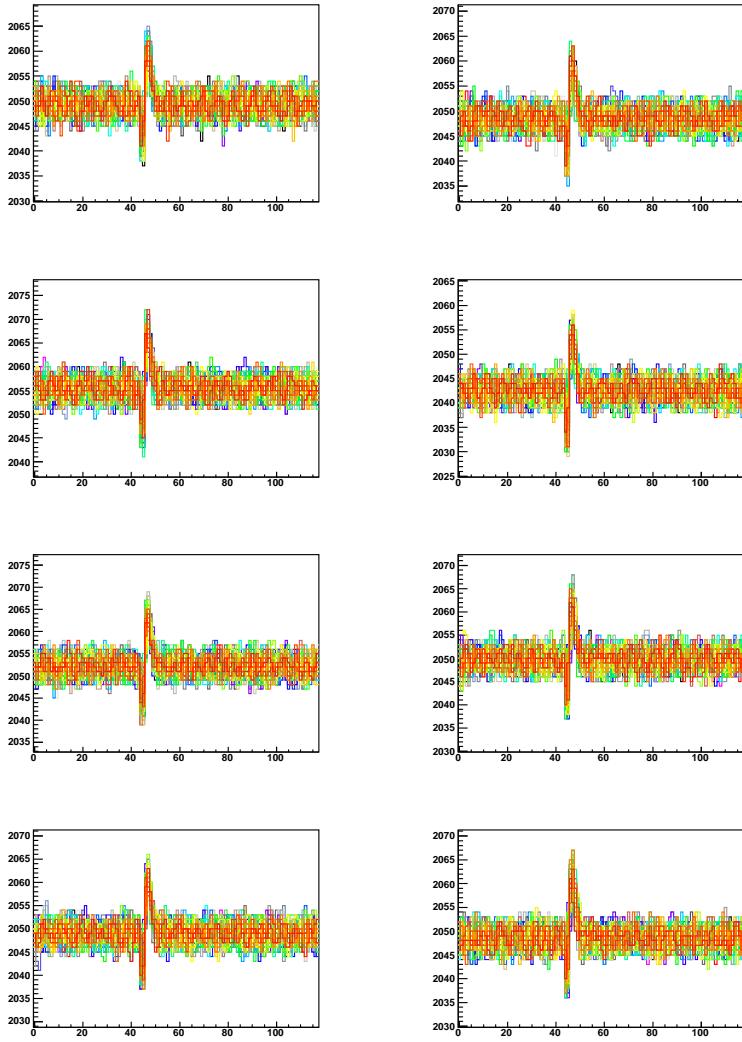


Figure 34: Channel-to-channel crosstalk of channels 9-16 for ASIC chip 2 with channel 1 unmasked (corresponding to FEM7 channels 24-31 with channel 16 unmasked). A 600 mV test pulse is sent to each ASIC chip. Note this is for induction wire ADC baseline.

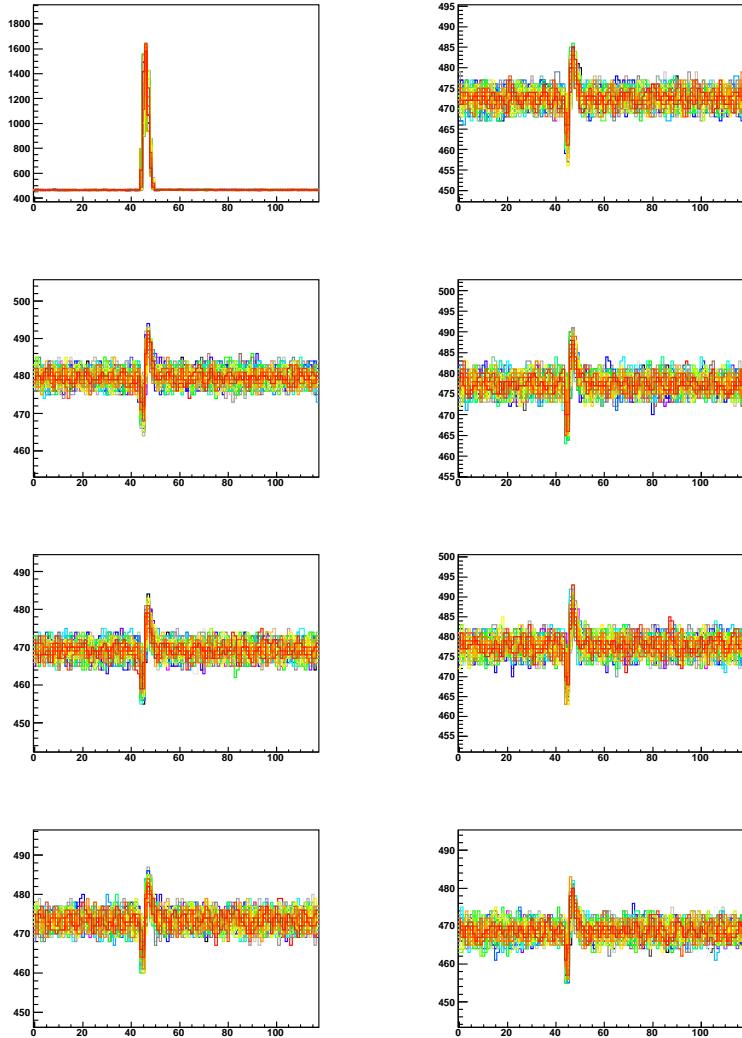


Figure 35: Channel-to-channel crosstalk of channels 1-8 for ASIC chip 1 with channel 1 unmasked (corresponding to FEM7 channels 32-39 with channel 32 unmasked). A 600 mV test pulse is sent to each ASIC chip. Note this is for collection wire ADC baseline.

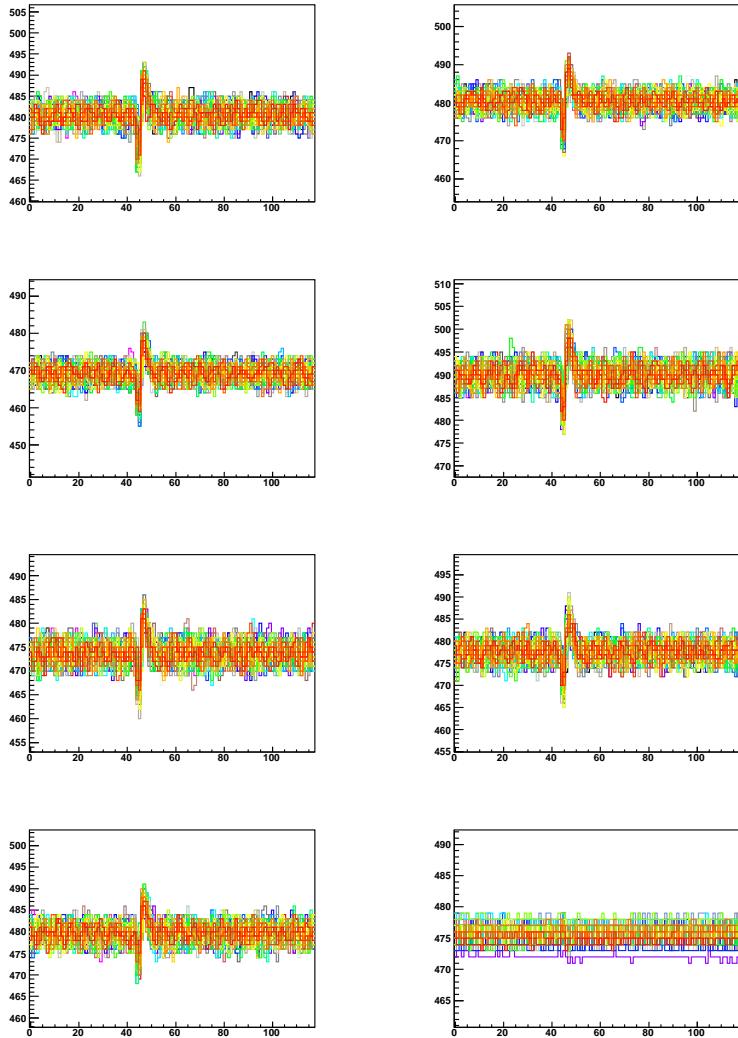


Figure 36: Channel-to-channel crosstalk of channels 9-16 for ASIC chip 1 with channel 1 unmasked (corresponding to FEM7 channels 40-47 with channel 32 unmasked). A 600 mV test pulse is sent to each ASIC chip. Note this is for collection wire ADC baseline.

0.9% the height of the original pulsed collection wire channels (11 ADC values from baseline for crosstalk peak compared to 1200 ADC values above baseline for pulsed peak). The chip-to-chip crosstalk on another collection wire ASIC is also a negative ADC peak followed by a tiny positive ADC valued peak with both peaks roughly the same deviation from baseline. Each of the collection wire ASIC channel peaks has a height about 1.0% the height of the original pulsed collection wire channels (12 ADC values from baseline for crosstalk peak compared to 1200 ADC values above baseline for pulsed peak).

For an induction wire ASIC that is pulsed (600 mV test pulse), the chip-to-chip crosstalk on another collection wire ASIC is a negative ADC peak followed by a tiny positive ADC valued peak with both peaks roughly the same deviation from baseline. Each of the conduction wire ASIC channel peaks has a height about 1.25% the height of the original pulsed induction wire channels (15 ADC values from baseline for crosstalk peak compared to 1200 ADC values above baseline for pulsed peak). The chip-to-chip crosstalk on another induction wire ASIC is a tiny positive ADC valued peak with a height about 0.75% the height of the original pulsed induction wire ASIC channel (9 ADC values above baseline for crosstalk peak compared to 1200 ADC values above baseline for pulsed peak).

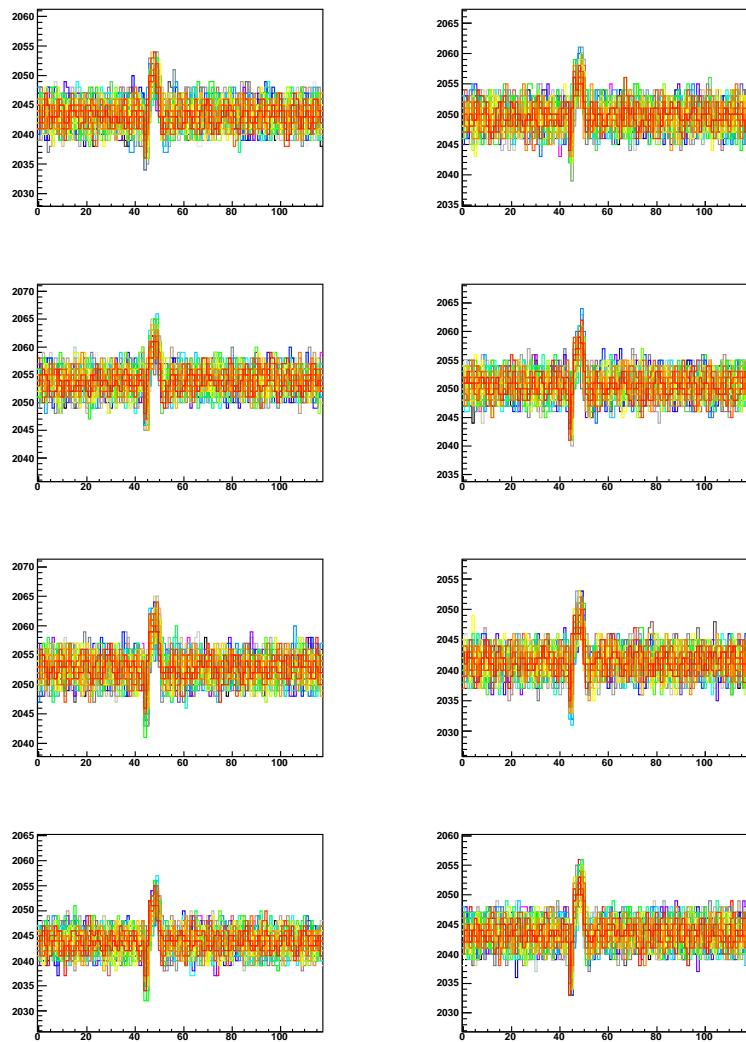


Figure 37: Crosstalk signals in channels 1-8 for ASIC 2 when ASIC 1 is unmasked and ASIC 2 is masked. A 600 mV test pulse is used.

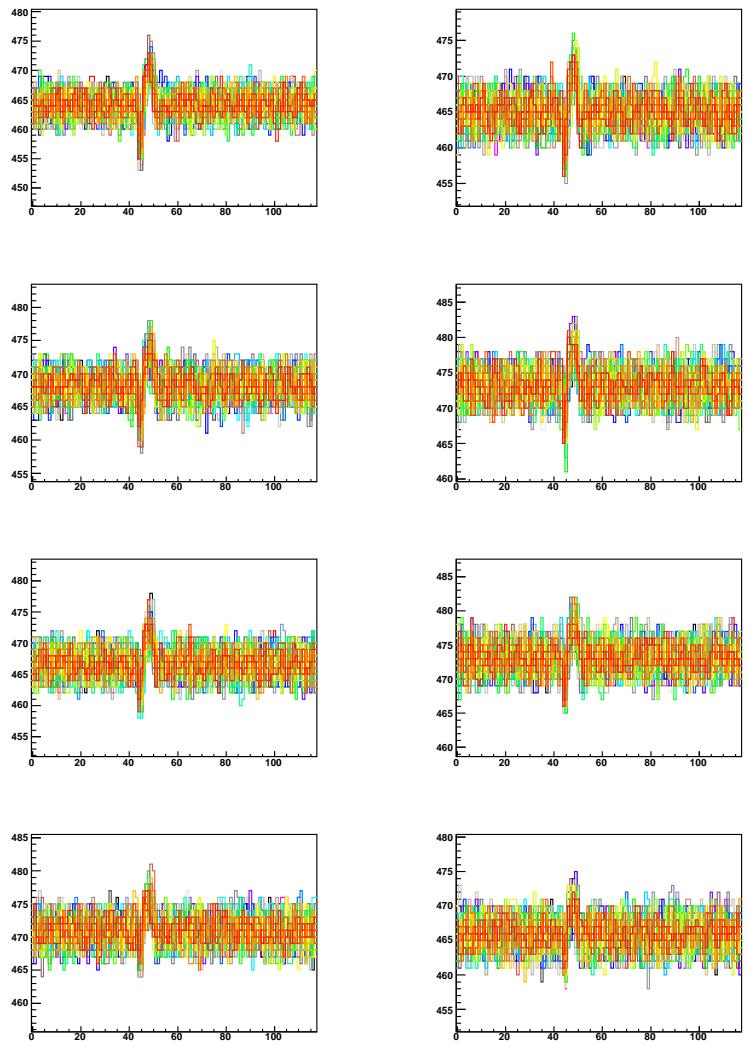


Figure 38: Crosstalk signals in channels 1-8 for ASIC 3 when ASIC 1 is unmasked and ASIC 3 is masked. A 600 mV test pulse is used.

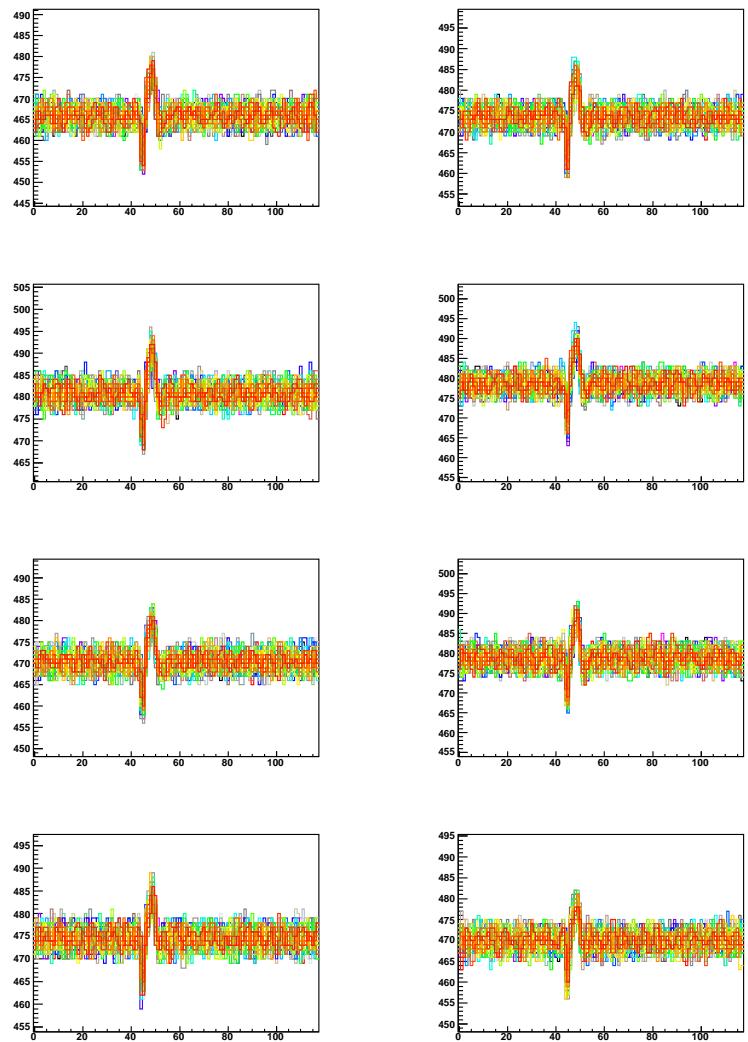


Figure 39: Crosstalk signals in channels 1-8 for ASIC 1 when ASIC 2 is unmasked and ASIC 1 is masked. A 600 mV test pulse is used.

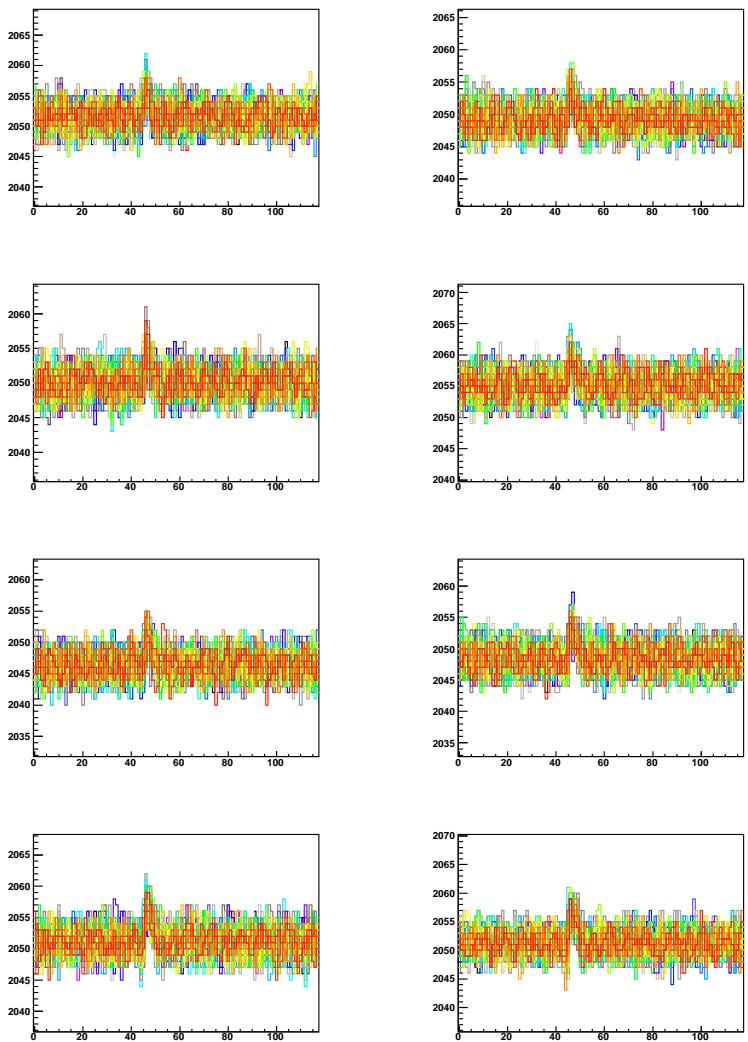


Figure 40: Crosstalk signals in channels 1-8 for ASIC 4 when ASIC 2 is unmasked and ASIC 4 is masked. A 600 mV test pulse is used.

7 Appendix A: ADC Values and Resolutions with 600 mV Pulse

A typical particle induces charge on the induction and collection wires that corresponds to roughly a 600 mV test pulse. Tables 1 to 12 show the max ADC value (V_{max}) resolution and initial time resolution (t_{max}) for 1000 events using a 600 mV test pulse for all FEMs.

Table 1: V_{max} (ADC value) and t_{max} (ticks) resolutions (RMS) for all channels (0-63) in FEM1. 1000 events are used with a 600 mV test pulse.

Ch #	V_{max} RMS	t_{max} RMS	Ch #	V_{max} RMS	t_{max} RMS
0	35.463266	0.335200	32	33.153713	0.335200
1	36.016807	0.335200	33	33.221340	0.335200
2	36.488874	0.335200	34	33.231419	0.335200
3	36.484430	0.335200	35	33.731836	0.335200
4	36.963164	0.335200	36	33.399730	0.335200
5	37.092444	0.335200	37	33.271691	0.335200
6	37.648644	0.335200	38	33.179177	0.335200
7	37.243314	0.335200	39	33.163353	0.335200
8	36.976129	0.335200	40	33.684702	0.335200
9	37.878874	0.335200	41	33.366577	0.335200
10	37.705045	0.335200	42	33.477314	0.335200
11	38.090210	0.335200	43	33.460559	0.335200
12	37.988994	0.338491	44	33.168727	0.335200
13	38.331800	0.338491	45	1.166883	0.339575
14	38.889807	0.427690	46	33.368457	0.335200
15	38.428064	0.437534	47	33.697267	0.335200
16	33.965451	0.335200	48	35.784940	0.335200
17	34.137501	0.335200	49	37.674145	0.335200
18	34.258477	0.335200	50	37.065999	0.335200
19	34.209933	0.335200	51	37.739316	0.335200
20	34.555478	0.335200	52	37.051546	0.335200
21	34.788758	0.335200	53	36.525651	0.335200
22	34.309842	0.335200	54	38.039456	0.335200
23	34.428621	0.335200	55	38.392996	0.335200
24	34.499074	0.335200	56	37.361344	0.335200
25	34.664356	0.335200	57	38.917450	0.364741
26	34.757002	0.335200	58	37.820150	0.335200
27	34.690306	0.335200	59	37.632889	0.335200
28	0.433450	27.885277	60	37.901292	0.335200
29	34.961351	0.335200	61	38.008735	0.335200
30	34.694810	0.335200	62	38.706276	0.433589
31	34.916873	0.335200	63	38.273977	0.437534

Table 2: V_{max} (ADC value) and t_{max} (ticks) resolutions (RMS) for all channels (0-63) in FEM2. 1000 events are used with a 600 mV test pulse.

Ch #	V_{max} RMS	t_{max} RMS	Ch #	V_{max} RMS	t_{max} RMS
0	33.391155	0.335200	32	35.767239	0.335200
1	33.440710	0.335200	33	35.792789	0.335200
2	33.451024	0.335200	34	36.510713	0.335200
3	33.722254	0.335200	35	36.206435	0.335200
4	33.840944	0.335200	36	36.724338	0.335200
5	33.380620	0.335200	37	36.516679	0.335200
6	33.553978	0.335200	38	37.039929	0.335200
7	33.466371	0.335200	39	37.509706	0.335200
8	33.301018	0.335200	40	36.223969	0.335200
9	33.401512	0.335200	41	37.797249	0.335200
10	33.330812	0.335200	42	36.469724	0.335200
11	33.235610	0.335200	43	36.779928	0.335200
12	33.452758	0.335200	44	38.692357	0.377380
13	33.432790	0.335200	45	38.049845	0.343847
14	33.651910	0.335200	46	37.450195	0.335200
15	33.956613	0.335200	47	0.332925	2.303398
16	34.394296	0.335200	48	33.154370	0.335200
17	34.484513	0.335200	49	33.171767	0.335200
18	34.643226	0.335200	50	33.256941	0.335200
19	34.405011	0.335200	51	33.309612	0.335200
20	34.881864	0.335200	52	33.115088	0.335200
21	34.824560	0.335200	53	33.210330	0.335200
22	35.093133	0.335200	54	33.167633	0.335200
23	35.036123	0.335200	55	33.388104	0.335200
24	35.039338	0.335200	56	33.426310	0.335200
25	35.133281	0.335200	57	33.503572	0.335200
26	35.577403	0.335200	58	33.620827	0.335200
27	35.279275	0.335200	59	33.515726	0.335200
28	35.435683	0.335200	60	33.482395	0.335200
29	35.980000	0.335200	61	33.412297	0.335200
30	35.834015	0.335200	62	33.408740	0.335200
31	36.118661	0.335200	63	1.557472	0.438634

Table 3: V_{max} (ADC value) and t_{max} (ticks) resolutions (RMS) for all channels (0-63) in FEM3. 1000 events are used with a 600 mV test pulse.

Ch #	V_{max} RMS	t_{max} RMS	Ch #	V_{max} RMS	t_{max} RMS
0	38.358370	0.353106	32	33.314935	0.335200
1	38.752327	0.405877	33	33.214393	0.335200
2	38.346035	0.437534	34	33.755187	0.335200
3	38.283112	0.437534	35	33.567199	0.335200
4	38.400933	0.437534	36	33.514633	0.335200
5	38.298796	0.437534	37	33.412074	0.335200
6	38.248083	0.437534	38	33.582284	0.335200
7	38.067177	0.437534	39	33.765030	0.335200
8	38.054991	0.437534	40	33.595385	0.335200
9	38.202308	0.437534	41	33.491146	0.335200
10	37.662244	0.437534	42	33.455731	0.335200
11	37.653948	0.437534	43	33.879576	0.335200
12	37.491103	0.437534	44	33.664906	0.335200
13	37.351543	0.437534	45	33.624467	0.335200
14	37.723571	0.437534	46	33.692530	0.335200
15	37.274548	0.437534	47	0.503313	0.496740
16	36.997077	0.335200	48	35.963035	0.335200
17	37.400676	0.335200	49	35.526787	0.335200
18	54.822109	0.437534	50	35.732942	0.335200
19	38.209149	0.341724	51	36.290948	0.335200
20	38.217385	0.337400	52	35.950443	0.335200
21	38.225701	0.348022	53	36.548350	0.335200
22	38.676233	0.391509	54	36.091715	0.335200
23	38.420074	0.366606	55	35.697168	0.335200
24	38.913522	0.382513	56	36.018801	0.335200
25	38.831881	0.399248	57	36.587045	0.335200
26	38.602925	0.434731	58	36.029856	0.335200
27	38.601627	0.436979	59	36.513104	0.335200
28	38.419628	0.436422	60	37.168553	0.335200
29	37.971061	0.437534	61	36.964858	0.335200
30	37.895575	0.437534	62	36.544109	0.335200
31	38.221739	0.437534	63	2.256489	0.483864

Table 4: V_{max} (ADC value) and t_{max} (ticks) resolutions (RMS) for all channels (0-63) in FEM4. 1000 events are used with a 600 mV test pulse.

Ch #	V_{max} RMS	t_{max} RMS	Ch #	V_{max} RMS	t_{max} RMS
0	35.063168	0.335200	32	34.499401	0.335200
1	35.151734	0.335200	33	35.873579	0.335200
2	35.336333	0.335200	34	35.699775	0.335200
3	35.449302	0.335200	35	35.846131	0.335200
4	35.384336	0.335200	36	35.526139	0.335200
5	35.460170	0.335200	37	36.227059	0.335200
6	35.405760	0.335200	38	36.865189	0.335200
7	35.286778	0.335200	39	36.017796	0.335200
8	35.321938	0.335200	40	36.561912	0.335200
9	35.259267	0.335200	41	36.648727	0.335200
10	35.198871	0.335200	42	38.527531	0.367531
11	35.755470	0.335200	43	37.057734	0.335200
12	35.709306	0.335200	44	37.700111	0.335200
13	35.791583	0.335200	45	38.115924	0.340652
14	36.398763	0.335200	46	38.364823	0.339575
15	36.342398	0.335200	47	38.306889	0.374752
16	35.830467	0.335200	48	37.545999	0.335200
17	36.233310	0.335200	49	38.145991	0.391509
18	36.271819	0.335200	50	38.216324	0.353106
19	36.114676	0.335200	51	38.545319	0.428294
20	36.389199	0.335200	52	37.720513	0.339575
21	36.434492	0.335200	53	37.541768	0.335200
22	36.573453	0.335200	54	37.542096	0.335200
23	35.888557	0.335200	55	38.074397	0.437534
24	36.515498	0.335200	56	38.384283	0.343847
25	36.793458	0.335200	57	38.196528	0.412203
26	36.820625	0.335200	58	38.388258	0.434161
27	37.050803	0.335200	59	38.204988	0.436979
28	36.835225	0.335200	60	37.753335	0.437534
29	37.421998	0.335200	61	38.168955	0.437534
30	37.227493	0.335200	62	38.153575	0.396201
31	29.779827	0.335200	63	37.582168	0.437534

Table 5: V_{max} (ADC value) and t_{max} (ticks) resolutions (RMS) for all channels (0-63) in FEM5. 1000 events are used with a 600 mV test pulse.

Ch #	V_{max} RMS	t_{max} RMS	Ch #	V_{max} RMS	t_{max} RMS
0	33.311762	0.335200	32	33.150282	0.335200
1	33.870716	0.335200	33	33.283913	0.335200
2	33.670374	0.335200	34	33.352481	0.335200
3	34.306508	0.335200	35	33.336471	0.335200
4	33.879168	0.335200	36	33.422609	0.335200
5	34.153763	0.335200	37	33.501976	0.335200
6	34.562761	0.335200	38	33.456495	0.335200
7	34.207974	0.335200	39	33.501183	0.335200
8	34.381123	0.335200	40	33.590912	0.335200
9	34.449756	0.335200	41	33.706400	0.335200
10	35.105025	0.335200	42	33.718534	0.335200
11	34.442192	0.335200	43	33.570689	0.335200
12	35.649404	0.335200	44	33.719435	0.335200
13	36.627844	0.335200	45	33.599140	0.335200
14	35.917954	0.335200	46	34.122461	0.335200
15	35.560794	0.335200	47	34.261747	0.335200
16	33.085486	0.335200	48	37.712977	0.437534
17	33.276352	0.335200	49	37.748944	0.437534
18	33.494762	0.335200	50	37.025957	0.437534
19	33.414258	0.335200	51	37.438179	0.437534
20	33.303861	0.335200	52	37.418201	0.437534
21	33.262819	0.335200	53	37.250638	0.437534
22	33.310884	0.335200	54	37.184810	0.437534
23	33.404178	0.335200	55	37.462166	0.437534
24	33.715860	0.335200	56	37.323947	0.437534
25	33.574814	0.335200	57	37.138692	0.437534
26	33.399535	0.335200	58	37.108978	0.437534
27	33.832685	0.335200	59	37.274993	0.437534
28	34.472585	0.335200	60	37.094088	0.437534
29	33.850775	0.335200	61	36.957438	0.437534
30	34.452099	0.335200	62	36.800819	0.437534
31	33.818231	0.335200	63	36.868884	0.437534

Table 6: V_{max} (ADC value) and t_{max} (ticks) resolutions (RMS) for all channels (0-63) in FEM6. 1000 events are used with a 600 mV test pulse.

Ch #	V_{max} RMS	t_{max} RMS	Ch #	V_{max} RMS	t_{max} RMS
0	38.622698	0.362855	32	38.235465	0.339575
1	38.366330	0.420833	33	38.559581	0.393089
2	38.365005	0.436422	34	38.042249	0.437534
3	38.342643	0.436979	35	38.539778	0.430087
4	38.308090	0.437534	36	38.601679	0.362855
5	38.114728	0.437534	37	38.367414	0.335200
6	38.555752	0.437534	38	38.844356	0.413569
7	37.950004	0.437534	39	38.047659	0.437534
8	37.763581	0.437534	40	38.134203	0.437534
9	37.566752	0.437534	41	38.546776	0.437534
10	37.451619	0.437534	42	39.203197	0.435861
11	37.339458	0.437534	43	37.686138	0.437534
12	37.637881	0.437534	44	38.567271	0.437534
13	37.375687	0.437534	45	37.007830	0.437534
14	37.419780	0.437534	46	36.712351	0.437534
15	0.520554	0.321988	47	0.596470	0.499900
16	35.568692	0.335200	48	39.003208	0.392301
17	36.041451	0.335200	49	38.408546	0.437534
18	35.878204	0.335200	50	39.444865	0.423999
19	35.632434	0.335200	51	39.136211	0.378247
20	36.095909	0.335200	52	38.791386	0.340652
21	35.877015	0.335200	53	38.850819	0.376509
22	7.495539	0.000000	54	38.986254	0.437534
23	0.251746	15.516760	55	38.483211	0.437534
24	36.183037	0.335200	56	39.002423	0.389912
25	36.453035	0.335200	57	37.460526	0.437534
26	36.029412	0.335200	58	39.249223	0.379109
27	36.165660	0.335200	59	37.851968	0.437534
28	36.924801	0.335200	60	37.016033	0.437534
29	36.345121	0.335200	61	37.179970	0.437534
30	36.617849	0.335200	62	38.211384	0.437534
31	0.393705	0.450351	63	0.387266	0.483271

Table 7: V_{max} (ADC value) and t_{max} (ticks) resolutions (RMS) for all channels (0-63) in FEM7. 1000 events are used with a 600 mV test pulse.

Ch #	V_{max} RMS	t_{max} RMS	Ch #	V_{max} RMS	t_{max} RMS
0	39.816154	0.350073	32	35.987904	0.335200
1	39.520758	0.436422	33	35.997380	0.335200
2	39.906570	0.428294	34	36.036665	0.335200
3	39.459897	0.437534	35	36.544574	0.335200
4	38.949048	0.437534	36	36.513179	0.335200
5	39.021891	0.437534	37	36.789627	0.335200
6	39.415865	0.437534	38	36.625792	0.335200
7	38.417619	0.437534	39	36.710700	0.335200
8	40.300685	0.434731	40	36.569303	0.335200
9	40.528093	0.434731	41	36.805391	0.335200
10	39.282864	0.437534	42	36.985771	0.335200
11	39.909586	0.437534	43	37.422010	0.335200
12	38.525783	0.437534	44	37.897932	0.335200
13	39.902202	0.408725	45	37.418771	0.335200
14	39.397364	0.437534	46	37.992557	0.335200
15	39.304995	0.437534	47	2.572815	16.946433
16	36.524038	0.335200	48	35.575232	0.335200
17	36.754498	0.335200	49	36.234056	0.335200
18	35.802602	0.335200	50	35.965553	0.335200
19	36.490912	0.335200	51	36.403443	0.335200
20	37.058885	0.335200	52	36.588019	0.335200
21	37.070046	0.335200	53	36.963344	0.335200
22	37.220740	0.335200	54	37.240890	0.335200
23	36.747044	0.335200	55	37.007008	0.335200
24	36.552448	0.335200	56	37.553845	0.335200
25	37.205089	0.335200	57	37.504618	0.335200
26	36.913427	0.335200	58	38.453087	0.335200
27	38.416137	0.335200	59	38.625454	0.335200
28	37.364582	0.335200	60	38.475160	0.335200
29	36.631145	0.335200	61	39.250794	0.335200
30	37.192819	0.335200	62	38.920850	0.335200
31	37.386527	0.335200	63	38.978826	0.336303

Table 8: V_{max} (ADC value) and t_{max} (ticks) resolutions (RMS) for all channels (0-63) in FEM8. 1000 events are used with a 600 mV test pulse.

Ch #	V_{max} RMS	t_{max} RMS	Ch #	V_{max} RMS	t_{max} RMS
0	34.298850	0.335200	32	36.403505	0.335200
1	34.409566	0.335200	33	36.800508	0.335200
2	34.221712	0.335200	34	37.444449	0.335200
3	34.667995	0.335200	35	37.652034	0.335200
4	34.557870	0.335200	36	37.941842	0.335200
5	34.558829	0.335200	37	38.188911	0.335200
6	34.086695	0.335200	38	38.090657	0.335200
7	34.407228	0.335200	39	37.996825	0.335200
8	34.600094	0.335200	40	38.747036	0.335200
9	34.249234	0.335200	41	39.710195	0.341724
10	34.705612	0.335200	42	39.908687	0.372081
11	34.636885	0.335200	43	40.136049	0.405156
12	34.205649	0.335200	44	39.834733	0.432434
13	34.776092	0.335200	45	39.238517	0.437534
14	34.867621	0.335200	46	39.090149	0.437534
15	34.753818	0.335200	47	39.118341	0.437534
16	34.783678	0.335200	48	39.493421	0.335200
17	35.217050	0.335200	49	39.709946	0.344900
18	35.695624	0.335200	50	39.840863	0.426473
19	35.720128	0.335200	51	39.833952	0.436422
20	35.961674	0.335200	52	39.653197	0.436422
21	35.734115	0.335200	53	39.589865	0.437534
22	35.629684	0.335200	54	39.228055	0.437534
23	35.571893	0.335200	55	39.632237	0.437534
24	35.082157	0.335200	56	39.357926	0.437534
25	36.069466	0.335200	57	39.466010	0.437534
26	35.485105	0.335200	58	39.714254	0.437534
27	36.269662	0.335200	59	39.497529	0.437534
28	36.257375	0.335200	60	39.088195	0.437534
29	35.807193	0.335200	61	38.623164	0.437534
30	36.193404	0.335200	62	38.270043	0.437534
31	1.478437	0.488635	63	38.595030	0.437534

8 Appendix B: Linearity Tests: Slope and Intercept Values

9 Appendix C: AFG3252 Configuration

The AFG3252 configuration files control the magnitude of the input pulse voltage the wire signals. There are two sets of AFG3252 configuration files,

Table 9: V_{max} (ADC value) and t_{max} (ticks) resolutions (RMS) for all channels (0-63) in FEM9. 1000 events are used with a 600 mV test pulse.

Ch #	V_{max} RMS	t_{max} RMS	Ch #	V_{max} RMS	t_{max} RMS
0	39.480062	0.377380	32	36.309296	0.335200
1	39.573754	0.346987	33	37.080343	0.335200
2	39.355546	0.436979	34	37.470843	0.335200
3	39.723259	0.407308	35	37.490652	0.335200
4	39.759044	0.355100	36	37.727021	0.335200
5	38.904207	0.437534	37	38.070028	0.335200
6	39.821214	0.422109	38	37.978328	0.335200
7	39.782659	0.431852	39	38.195638	0.335200
8	40.058914	0.426473	40	38.320787	0.335200
9	39.827843	0.404430	41	38.937264	0.335200
10	39.152261	0.437534	42	38.820042	0.335200
11	39.602920	0.437534	43	39.771396	0.343847
12	38.897990	0.437534	44	39.529140	0.353106
13	39.653240	0.436422	45	39.526221	0.353106
14	39.083033	0.437534	46	40.406689	0.411514
15	38.304964	0.437534	47	0.516898	0.467059
16	34.695655	0.335200	48	37.714679	0.335200
17	34.465813	0.335200	49	38.588997	0.335200
18	34.603231	0.335200	50	38.702200	0.335200
19	35.033089	0.335200	51	38.665462	0.335200
20	34.312721	0.335200	52	39.376251	0.335200
21	34.710383	0.335200	53	39.106493	0.336303
22	35.294584	0.335200	54	39.270901	0.335200
23	35.194128	0.335200	55	39.247545	0.335200
24	34.691667	0.335200	56	39.140590	0.335200
25	34.978149	0.335200	57	40.142730	0.353106
26	35.557790	0.335200	58	39.811381	0.338491
27	34.961774	0.335200	59	39.719433	0.382513
28	35.383434	0.335200	60	39.798370	0.435861
29	35.113211	0.335200	61	39.914757	0.433589
30	0.318094	21.531233	62	39.431978	0.434161
31	36.031110	0.335200	63	39.819108	0.433589

AFG3252 (which includes the executable file **myconfigafg3252** created using **makefile** from the settings of **myconfigafg3252.c** file) and AFG3252_secondchannel (which includes the executable file **myconfigafg3252_secondchannel** created using **makefile_secondchannel** from the settings of **myconfigafg3252_secondchannel.c** file), and each controls half of the wire signals in the prototype test stand. The files are located in the MicroBooNE DAQ repository on Redmine at:

Table 10: V_{max} (ADC value) and t_{max} (ticks) resolutions (RMS) for all channels (0-63) in FEM10. 1000 events are used with a 600 mV test pulse.

Ch #	V_{max} RMS	t_{max} RMS	Ch #	V_{max} RMS	t_{max} RMS
0	37.147144	0.335200	32	34.817012	0.335200
1	36.827558	0.335200	33	35.207497	0.335200
2	37.742266	0.335200	34	35.299040	0.335200
3	37.276931	0.335200	35	35.480341	0.335200
4	37.636073	0.335200	36	35.177326	0.335200
5	36.837489	0.335200	37	35.844439	0.335200
6	36.741080	0.335200	38	35.861228	0.335200
7	37.022165	0.335200	39	36.117612	0.335200
8	37.495359	0.335200	40	36.305516	0.335200
9	36.296325	0.335200	41	36.017988	0.335200
10	36.724465	0.335200	42	36.478493	0.335200
11	37.404294	0.335200	43	36.782552	0.335200
12	37.127476	0.335200	44	36.926335	0.335200
13	36.754762	0.335200	45	36.844531	0.335200
14	36.367595	0.335200	46	37.278185	0.335200
15	37.448957	0.335200	47	37.351416	0.335200
16	35.759170	0.335200	48	39.570067	0.434161
17	37.070495	0.335200	49	39.115591	0.437534
18	37.282334	0.335200	50	39.359001	0.437534
19	35.717852	0.335200	51	38.921258	0.437534
20	37.239982	0.335200	52	38.607983	0.437534
21	36.301482	0.335200	53	38.485807	0.437534
22	36.066181	0.335200	54	38.553411	0.437534
23	36.167269	0.335200	55	38.412719	0.437534
24	36.481542	0.335200	56	38.513236	0.437534
25	36.814535	0.335200	57	38.749921	0.437534
26	36.041632	0.335200	58	38.297779	0.437534
27	37.265036	0.335200	59	38.042307	0.437534
28	37.467821	0.335200	60	38.097735	0.437534
29	37.028079	0.335200	61	37.788975	0.437534
30	36.911669	0.335200	62	37.845163	0.437534
31	37.523068	0.335200	63	37.361408	0.437534

<https://cdcvn.fnal.gov/redmine/projects/uboonedaq/repository/revisions/cetcmake/show/projects/dabwork/calibration/GPIB-AFG3252>

First, the executables **myconfigafg3252** and **myconfigafg3252_secondchannel** must be created by running **makefile** (reading in the configuration file **myconfigafg3252.c**) and **makefile_secondchannel** (reading in the configuration

Table 11: V_{max} (ADC value) and t_{max} (ticks) resolutions (RMS) for all channels (0-63) in FEM11. 1000 events are used with a 600 mV test pulse.

Ch #	V_{max} RMS	t_{max} RMS	Ch #	V_{max} RMS	t_{max} RMS
0	36.529084	0.335200	32	34.675905	0.335200
1	37.638207	0.335200	33	35.071299	0.335200
2	36.574158	0.335200	34	35.180732	0.335200
3	36.849667	0.335200	35	35.078695	0.335200
4	36.319889	0.335200	36	35.094030	0.335200
5	37.517665	0.335200	37	35.868638	0.335200
6	36.597958	0.335200	38	35.671422	0.335200
7	37.328338	0.335200	39	35.799017	0.335200
8	38.067198	0.335200	40	36.369697	0.335200
9	38.931602	0.335200	41	36.372145	0.335200
10	38.096924	0.335200	42	36.412605	0.335200
11	39.304063	0.337400	43	37.073536	0.335200
12	39.104073	0.336303	44	36.999965	0.335200
13	38.096498	0.335200	45	36.990676	0.335200
14	39.327629	0.367531	46	37.737590	0.335200
15	39.248999	0.371181	47	37.008285	0.335200
16	37.807130	0.335200	48	36.669854	0.335200
17	37.595731	0.335200	49	37.347144	0.335200
18	38.136848	0.335200	50	37.583103	0.335200
19	38.935521	0.335200	51	37.246414	0.335200
20	39.775379	0.409428	52	37.858277	0.335200
21	37.565345	0.335200	53	37.675426	0.335200
22	39.344130	0.349050	54	37.843251	0.335200
23	38.777833	0.335200	55	37.716895	0.335200
24	38.923490	0.335200	56	37.695054	0.335200
25	39.162821	0.345947	57	38.335664	0.335200
26	38.369624	0.335200	58	38.498480	0.335200
27	39.835311	0.433013	59	38.330028	0.335200
28	39.452782	0.436979	60	38.569345	0.335200
29	39.496560	0.434161	61	39.345960	0.340652
30	40.041331	0.426473	62	38.793274	0.335200
31	0.089353	13.953663	63	39.072795	0.340652

file **myconfigafg3252_secondchannel.c**), respectively. To set the input pulse voltage for AFG3252, the voltage settings must first be cleared for AFG3252 by typing `./myconfigafg3252 -a voltage -o 0` in the directory of the **myconfigafg3252** executable file, where *voltage* is the desired input pulse voltage in V. The process must be repeated to set the input pulse voltage for AFG3252_secondchannel and the voltage settings must again first be cleared

Table 12: V_{max} (ADC value) and t_{max} (ticks) resolutions (RMS) for all channels (0-63) in FEM12. 1000 events are used with a 600 mV test pulse.

Ch #	V_{max} RMS	t_{max} RMS	Ch #	V_{max} RMS	t_{max} RMS
0	34.389798	0.335200	32	39.367828	0.436979
1	33.999453	0.335200	33	38.983664	0.437534
2	34.209619	0.335200	34	38.523840	0.437534
3	33.975398	0.335200	35	38.352632	0.437534
4	34.324795	0.335200	36	38.770910	0.437534
5	34.438860	0.335200	37	38.706898	0.437534
6	33.940405	0.335200	38	38.459567	0.437534
7	34.243726	0.335200	39	37.717804	0.437534
8	34.408542	0.335200	40	38.115681	0.437534
9	34.344093	0.335200	41	38.016455	0.437534
10	34.449538	0.335200	42	38.303432	0.437534
11	34.289502	0.335200	43	38.330797	0.437534
12	34.301492	0.335200	44	38.061799	0.437534
13	34.287511	0.335200	45	37.772669	0.437534
14	34.494330	0.335200	46	37.984628	0.437534
15	30.334456	0.335200	47	37.773259	0.437534
16	38.754198	0.437534	48	36.274247	0.335200
17	38.186884	0.437534	49	36.536617	0.335200
18	38.086021	0.437534	50	37.062132	0.335200
19	38.737814	0.437534	51	36.995486	0.335200
20	37.919789	0.437534	52	36.878205	0.335200
21	38.409790	0.437534	53	37.619931	0.335200
22	38.188197	0.437534	54	37.757954	0.335200
23	37.159043	0.437534	55	37.561309	0.335200
24	38.266597	0.437534	56	37.346212	0.335200
25	38.904770	0.437534	57	37.583036	0.335200
26	37.866316	0.437534	58	37.871957	0.335200
27	38.398095	0.437534	59	37.876336	0.335200
28	37.371751	0.437534	60	38.518152	0.335200
29	38.013578	0.437534	61	38.383844	0.335200
30	38.161262	0.437534	62	39.246215	0.335200
31	37.906355	0.437534	63	38.700431	0.335200

for AFG3252_secondchannel by typing `./myconfigafg3252_secondchannel -a voltage -o 0` in the directory of the `myconfigafg3252_secondchannel` executable file, where *voltage* is the desired input pulse voltage in V. The input pulse voltages can now be configured. For AFG3252, type `./myconfigafg3252 -a voltage` in the directory of the `myconfigafg3252` executable file, where *voltage* is the desired input pulse voltage in V. For AFG3252_secondchannel,

Table 13: Linear fit (using points from figure 15) with slope and intercept for all channels in FEM1.

Channel	Slope	Intercept	Channel	Slope	Intercept
0	1931.51	2049.33	32	1920.57	473.885
1	1934.37	2046.69	33	1927.3	470.973
2	1935.79	2044.28	34	1933.19	483.087
3	1930.39	2043.23	35	1965.62	466.835
4	1932.62	2057.8	36	1940.45	478.52
5	1930.24	2048.65	37	1936.04	460.015
6	1940.01	2040.11	38	1926	465.826
7	1935.02	2051.88	39	1935.99	466.746
8	1929.22	2044.96	40	1921.31	471.674
9	1926.53	2050.34	41	1939.67	468.821
10	1937.6	2047.43	42	1932.55	478.088
11	1943.45	2051.15	43	1948.42	471.463
12	1912.24	2044.18	44	1944.47	474.282
13	1924.87	2056.54	45	-	-
14	1932.77	2049.35	46	1940.97	474.602
15	1916.71	2052.34	47	1934.49	466.029
16	1934.71	2044.35	48	1956.96	462.485
17	1936.24	2053.69	49	1938.23	459.887
18	1936.3	2044.61	50	1979.45	473.773
19	1934.03	2052.8	51	1970.66	460.195
20	1941.99	2042.3	52	1966.29	464.13
21	1945.73	2055.14	53	1986.6	456.668
22	1936.73	2047.16	54	1937.69	470.353
23	1936.16	2049.91	55	1950.49	453.315
24	1941.34	2042.04	56	1956.29	478.628
25	1945.27	2042.64	57	1935.32	472.029
26	1950.65	2050.71	58	1962.18	474.842
27	1953.58	2058.75	59	1945.6	472.003
28	-	-	60	1945.86	484.362
29	1931.38	2049.99	61	1956.67	463.145
30	1938.78	2037.39	62	1919.2	479.473
31	1936.04	2046.09	63	1923.39	472.424

type `./myconfigafg3252_secondchannel -a voltage` in the directory of the `myconfigafg3252_secondchannel` executable file, where `voltage` is the desired input pulse voltage in V.

Table 14: Linear fit (using points from figure 15) with slope and intercept for all channels in FEM2.

Channel	Slope	Intercept	Channel	Slope	Intercept
0	1931.92	2044.32	32	1934.35	457.843
1	1927.97	2044.36	33	1940	474.089
2	1939.39	2052.95	34	1937.21	467.22
3	1939.85	2045.41	35	1934.12	473.179
4	1952.01	2045.54	36	1940.96	465.667
5	1946.04	2051.43	37	1939.32	470.282
6	1948.49	2045.5	38	1937.03	465.377
7	1933.72	2053.84	39	1953.11	481.901
8	1930.75	2048.16	40	1941.79	473.575
9	1940.02	2049.83	41	1937.83	475.591
10	1929.13	2046.65	42	1952.04	462.984
11	1914.73	2053.26	43	1937.85	472.969
12	1923.69	2051.49	44	1924.11	472.664
13	1932.94	2052.01	45	1917.78	488.655
14	1930.84	2039.66	46	1944.39	468.973
15	1938.23	2045.24	47	-	-
16	1929.23	2040.43	48	1907.4	482.419
17	1944.42	2048.61	49	1924.33	482.859
18	1946.37	2049.53	50	1925.95	478.423
19	1941.84	2045.16	51	1934.07	482.923
20	1953.72	2049.42	52	1924.45	490.201
21	1935.22	2035.08	53	1917.8	480.933
22	1950.24	2052.17	54	1925.57	479.818
23	1944.24	2044.51	55	1940.8	487.656
24	1952.07	2038.5	56	1946.21	466.403
25	1949.91	2049.88	57	1959.9	467.738
26	1950.26	2053.12	58	1957.91	466.704
27	1943.35	2044.54	59	1937.32	466.93
28	1949.9	2047.87	60	1938.34	480.018
29	1942.51	2052.17	61	1948.81	470.083
30	1941.84	2046.71	62	1932.3	475.435
31	1939.67	2044.96	63	-	-

10 Appendix D: ASIC Configuration

Figure 41 show the physical setup of the 4 ASIC motherboards in the lower portion of the test stand with the Faraday cages removed. There are two ASIC motherboards next to each other on each side. The two sides are labeled A and B. The information from the ASICs are read out through the cable slots on top

Table 15: Linear fit (using points from figure 15) with slope and intercept for all channels in FEM3.

Channel	Slope	Intercept	Channel	Slope	Intercept
0	1922.89	2048.65	32	1920.28	478.335
1	1916.34	2044.79	33	1918.13	473.241
2	1917.16	2048.6	34	1931.35	465.497
3	1915.3	2048.38	35	1949.27	470.607
4	1923.36	2047.08	36	1947.1	462.405
5	1926.47	2049.87	37	1945.74	468.392
6	1927.12	2046.77	38	1969.36	464.722
7	1929.55	2053.29	39	1926.12	475.894
8	1926.1	2043.57	40	1927.58	476.803
9	1922.12	2048.36	41	1909.83	475.249
10	1921.21	2045.57	42	1927.55	478.545
11	1919.37	2048.93	43	1920.48	476.261
12	1916.25	2050.49	44	1923.1	475.57
13	1914.37	2041.7	45	1924.94	467.541
14	1944.04	2048.51	46	1945.89	471.941
15	1921.43	2046.12	47	-	-
16	1932.14	2044.36	48	1925.35	477.848
17	1911.44	2047.53	49	1955.03	470.641
18	2768.31	2018.76	50	1948.93	474.667
19	1918.91	2045.45	51	1938.81	463.245
20	1932.67	2044.83	52	1943.38	469.187
21	1912.04	2041.27	53	1944.65	473.987
22	1926.52	2053.55	54	1941.04	469.478
23	1922.18	2041.4	55	1958.08	463.35
24	1940.65	2044.18	56	1954.66	475.441
25	1935.32	2041.38	57	1947.24	461.457
26	1926.63	2046.13	58	1965.18	465.73
27	1932.92	2043.67	59	1934.16	469.58
28	1930.37	2051.88	60	1933.84	463.657
29	1924.19	2047.42	61	1935.29	467.692
30	1920.28	2051.94	62	1933.63	468.381
31	1928.26	2041.52	63	-	-

of each motherboard with a single cable slot reading out information for each ASIC. The top row of cable slots controls the inward facing (facing into the test stand) ASICs directly below the corresponding slots. The bottom row of cable slots controls the outward facing (facing out of the test stand and visible in figure 41) ASICs directly below the corresponding slots. All 48 ASICs are individually identified in the document through their respective slots numbers

Table 16: Linear fit (using points from figure 15) with slope and intercept for all channels in FEM4.

Channel	Slope	Intercept	Channel	Slope	Intercept
0	1928.53	2054.76	32	1943.74	472.14
1	1921.16	2051.65	33	1939.24	472.952
2	1925.61	2048.63	34	1933.77	467.885
3	1929.01	2049.05	35	1938.54	463.857
4	1920.97	2044.93	36	1928.93	473.017
5	1927.66	2047.45	37	1941.27	475.12
6	1936.34	2041.11	38	1924.52	477.542
7	1917.96	2047.24	39	1945.87	473.3
8	1926.83	2053.17	40	1941.5	471.017
9	1921.57	2046.3	41	1932.61	472.322
10	1920.36	2053.45	42	1934.46	477.97
11	1923.76	2041.91	43	1949.68	470.439
12	1915.94	2047.37	44	1922.08	465.394
13	1922.38	2049.05	45	1927.67	479.63
14	1925.96	2048.52	46	1947.3	478.036
15	1919.66	2050.02	47	1942.75	470.961
16	1925.49	2049.94	48	1917.08	471.406
17	1930.69	2044.95	49	1904.61	467.08
18	1923.74	2047.97	50	1919.48	478.288
19	1936.13	2051.57	51	1926.04	469.225
20	1935.65	2054.72	52	1923.38	480.288
21	1939.03	2046.71	53	1933.14	474.88
22	1936.15	2050.36	54	1941.51	475.601
23	1934.24	2043.55	55	1910.73	477.575
24	1955.67	2043.42	56	1936.74	463.36
25	1947.25	2043.21	57	1915.24	474.937
26	1941.34	2044.95	58	1929.77	469.264
27	1956.93	2039.82	59	1931.85	472.68
28	1947.98	2039.29	60	1921.67	471.029
29	1944.09	2051.14	61	1934.65	467.925
30	1943.11	2045.79	62	1940.2	474.264
31	1570.73	2042.22	63	1930.49	466.471

as labeled in figure 41.

Each ASIC has 16 independent channels serving a quarter of a single FEM's 64 channels (4 ASICs per FEM). Table 25 shows how the individual ASICs labeled through figure 41 correspond to FEM channels. The 16 channels of each ASIC can be independently masked (turned off) and unmasked (turned on) using 4 hexadecimal digits, where each hexadecimal digit controls 4 channels.

Table 17: Linear fit (using points from figure 16) with slope and intercept for all channels in FEM5.

Channel	Slope	Intercept	Channel	Slope	Intercept
0	1929.77	2049.87	32	1918.07	465.155
1	1920.46	2047.14	33	1942.43	469.822
2	1942.97	2047.05	34	1938.86	479.59
3	1938.91	2041.21	35	1928.14	478.099
4	1938.42	2047.82	36	1945.06	477.903
5	1933.97	2049.16	37	1951.7	473.207
6	1934.17	2048.56	38	1955.35	460.586
7	1939.85	2047.37	39	1963.03	467.754
8	1923.25	2048.6	40	1956.74	462.628
9	1937.93	2046.55	41	1959.6	466.618
10	1936.36	2048.71	42	1930.97	475.999
11	1930.29	2057.52	43	1971.16	477.525
12	1940.89	2047.13	44	1925.73	477.124
13	1930.36	2040.3	45	1914.46	460.697
14	1929.61	2044.39	46	1938.87	469.667
15	1934.86	2050.71	47	1940.79	463.302
16	1924.3	2051.07	48	1940.3	470.144
17	1927.59	2043.52	49	1926.33	478.381
18	1927.38	2045.59	50	1946.97	485.548
19	1928.04	2050.39	51	1959.48	483.237
20	1918.56	2047.97	52	1956.17	469.689
21	1929.93	2046.62	53	1941.67	469.318
22	1919.19	2039.04	54	1914.56	476.053
23	1926.93	2049.86	55	1940.06	470.816
24	1935.72	2048.63	56	1944.89	474.563
25	1927.83	2043.53	57	1962.45	467.013
26	1928.25	2038.49	58	1949.86	470.926
27	1945.03	2050.01	59	1938.93	469.454
28	1947.69	2047.09	60	1932.45	471.688
29	1944.6	2041.33	61	1940.24	466.425
30	1932.34	2041.55	62	1944.14	478.508
31	1925.55	2046.07	63	1937.94	456.926

Each hexadecimal digit can be translated into 4 binary digits corresponding to the state of the 4 channels, whether masked or unmasked.

The ASIC configuration files control which ASIC channels are masked/unmasked and the gain of the ASIC at 4 different settings and peaking time of the ASIC at 4 different settings. There are two sets of ASIC configuration files, **ASIC042312** (which includes the executable file **asic042312** created using **Makefile-042312**

Table 18: Linear fit (using points from figure 16) with slope and intercept for all channels in FEM6.

Channel	Slope	Intercept	Channel	Slope	Intercept
0	1945	2054.93	32	1933.1	480.695
1	1928.19	2050.78	33	1926.9	472.385
2	1928.05	2041.13	34	1923.57	476.297
3	1927.84	2043.25	35	1925.73	477.161
4	1932.95	2046.92	36	1948.6	476.07
5	1923.89	2045.35	37	1957.61	480.586
6	1962.64	2036.74	38	1953.96	480.13
7	1927.24	2051.46	39	1929.61	476.078
8	1936.58	2053.46	40	1938.69	478.598
9	1934.08	2047.05	41	1949.17	468.174
10	1930.8	2049.89	42	1966.15	474.169
11	1930.19	2046.47	43	1943.34	459.23
12	1931.98	2036.41	44	1961.37	474.399
13	1933.06	2047.15	45	1941.43	469.123
14	1935.91	2046.61	46	1941.34	470.902
15	-	-	47	-	-
16	1938.84	2039.85	48	1950.41	456.208
17	1952.53	2052.67	49	1937.6	459.511
18	1948.47	2051.93	50	1968.15	469.868
19	1945.48	2049.01	51	1966.64	465.316
20	1956.24	2050.67	52	1987.65	466.538
21	1946.46	2047.25	53	1975.29	460.178
22	1690.72	2451.69	54	1969.8	468.169
23	-	-	55	1957.69	461.4
24	1946.44	2046.65	56	1969.71	464.452
25	1955.4	2043.46	57	1938.95	472.218
26	1950.36	2055.6	58	1981.61	471.867
27	1958.01	2041.79	59	1945.2	465.545
28	1959	2046.26	60	1936.28	470.707
29	1952.56	2058.56	61	1945.46	470.718
30	1943.38	2049.32	62	1959.12	466.106
31	-	-	63	-	-

from the settings of **asic042312.c** file) and ASIC042312_secondset (which includes the executable file **asic042312_secondset** created using **Makefile-042312-secondset** from the settings of **asic042312_secondset.c** file), and each controls half of the ASICs (24 ASIC chips out of 48 ASIC chips), serving half of the FEMs, in the prototype test stand. The files are located in the MicroBooNE DAQ repository on Redmine at:

Table 19: Linear fit (using points from figure 16) with slope and intercept for all channels in FEM7.

Channel	Slope	Intercept	Channel	Slope	Intercept
0	1924.25	2049.18	32	1914.1	465.946
1	1903.99	2049.01	33	1907.62	474.548
2	1923.4	2048.84	34	1909.92	480.866
3	1906.1	2054.9	35	1922.35	479.131
4	1904.29	2045.98	36	1906.29	470.252
5	1917.33	2047.78	37	1917.12	479.762
6	1920.88	2050.39	38	1897.05	474.94
7	1886.52	2052.93	39	1922.74	469.183
8	1934.45	2045.21	40	1912.4	481.343
9	1928.08	2045.75	41	1925.01	481.179
10	1907.05	2055.59	42	1920.95	469.65
11	1922.17	2053.74	43	1920.14	490.281
12	1893.57	2053.67	44	1927.62	475.282
13	1917.11	2042.74	45	1917	477.952
14	1921.27	2048.71	46	1920.01	480.121
15	1917.84	2046.55	47	-	-
16	1920.44	2042.89	48	1912.84	464.484
17	1907.22	2049.97	49	1915.71	465.929
18	1915.68	2052.35	50	1904.15	467.138
19	1933.33	2048.97	51	1924.12	473.453
20	1927.03	2051.86	52	1903.87	466.92
21	1908.02	2041.49	53	1920.87	473.663
22	1915.19	2044.17	54	1912.26	471.077
23	1914.81	2043.02	55	1910.42	465.613
24	1915.69	2050.01	56	1922.81	458.848
25	1901.94	2050.38	57	1926.45	466.168
26	1936.2	2054.21	58	1917.91	470.647
27	1915.75	2043.84	59	1926.52	466.406
28	1919.43	2052.3	60	1919.95	483.011
29	1933.72	2048.37	61	1914.2	462.897
30	1908.15	2048.95	62	1918.46	466.516
31	1918.92	2049.09	63	1911.69	474.452

<https://cdcvn.fnal.gov/redmine/projects/uboonedaq/repository/revisions/cetcmake/show/projects/dabwork/calibration/USB-ASIC>

First, the executables **asic042312** and **asic042312_secondset** must be created by running **Makefile-042312** (reading in the configuration file **asic042312.c**) and **Makefile-042312-secondset** (reading in the configuration file **asic042312_secondset.c**),

Table 20: Linear fit (using points from figure 16) with slope and intercept for all channels in FEM8.

Channel	Slope	Intercept	Channel	Slope	Intercept
0	1908.64	2043.64	32	1897.75	478.304
1	1921.51	2045.96	33	1902.47	493.193
2	1921.76	2045.29	34	1897.11	477.37
3	1931.59	2044.99	35	1909.19	483.423
4	1937.72	2045.29	36	1904.27	474.998
5	1907.6	2046.52	37	1904.57	481.214
6	1914.83	2056.03	38	1902.92	472.352
7	1901.1	2042.1	39	1899.64	480.226
8	1937.69	2042.58	40	1913.84	475.166
9	1925.75	2034.35	41	1913.21	489.54
10	1937.55	2041.05	42	1915.14	478.728
11	1928.3	2048.68	43	1908.75	473.817
12	1912.43	2050.81	44	1911.3	479.897
13	1907.08	2045.33	45	1902.27	482.595
14	1935.39	2045.13	46	1910.08	472.638
15	1924.1	2040.4	47	1912.64	475.573
16	1916.62	2047.16	48	1908.43	486.721
17	1936.32	2046.85	49	1910.68	485.545
18	1937.85	2042.34	50	1907.83	476.744
19	1930.02	2049.84	51	1912.2	477.691
20	1935.6	2043.47	52	1911.07	474.16
21	1928.01	2046.09	53	1903.63	486.039
22	1932.25	2048.69	54	1901.61	475.18
23	1936.31	2050.16	55	1910.62	488.204
24	1921.34	2054.94	56	1906.19	487.312
25	1924.12	2049.96	57	1919.71	472.193
26	1943.85	2048.14	58	1925.75	476.364
27	1919.7	2053.7	59	1924.88	476.37
28	1937.72	2046.71	60	1919.32	475.955
29	1926.93	2046.08	61	1909.29	473.647
30	1929.93	2051.38	62	1905.65	465.265
31	-	-	63	1909.44	477.278

respectively. To keep all the channels controlled by **asic042312** (half of the ASICs) unmasked, run **asic042312 -v** where **-v** gives the on-screen verification option. To keep all the channels controlled by **asic042312_secondset** (half of the ASICs) unmasked, run **asic042312_secondset -v** where **-v** gives the on-screen verification option.

Each of the individual ASIC channels can be masked/unmasked using differ-

Table 21: Linear fit (using points from figure 17) with slope and intercept for all channels in FEM9.

Channel	Slope	Intercept	Channel	Slope	Intercept
0	1904.29	2044.27	32	1910.2	468.639
1	1920.72	2046.31	33	1915.06	471.136
2	1902.79	2056.77	34	1921.48	476.051
3	1913.57	2047.49	35	1916.31	472.837
4	1923.25	2045.25	36	1909.34	475.689
5	1907.87	2048.76	37	1912.62	480.981
6	1919.06	2042.04	38	1920.92	467.588
7	1921.74	2054.46	39	1914.79	467.993
8	1919.19	2043.3	40	1913.94	467.499
9	1926.87	2042.13	41	1914.58	474.938
10	1912.07	2053.69	42	1917.73	470.134
11	1916.73	2050.15	43	1922.87	470.196
12	1908.49	2055.17	44	1915.11	459.749
13	1922.8	2051.14	45	1918.59	464.875
14	1919.09	2049.21	46	1933.65	472.76
15	1898.28	2042.03	47	-	-
16	1915.19	2049.93	48	1910.19	475.526
17	1934.17	2052.62	49	1917.4	469.017
18	1912.1	2052.76	50	1916.7	468.857
19	1934.95	2046.04	51	1919.97	477.946
20	1923.46	2046.07	52	1918.33	469.303
21	1920.95	2044.1	53	1916.16	477.048
22	1912.2	2047.63	54	1916.8	477.519
23	1921.08	2048.86	55	1917.06	472.353
24	1931.84	2051.21	56	1920.46	474.118
25	1946.61	2047.53	57	1929.79	469.483
26	1914.12	2051.72	58	1937.98	467.012
27	1948.54	2043.56	59	1913.45	475.099
28	1917.27	2041.73	60	1919.44	463.67
29	1933.89	2043.47	61	1924.08	464.686
30	-	-	62	1910.17	461.802
31	1886.65	2049.82	63	1917.73	471.685

ent options on the command line. The channels in the first 24 ASIC chips (16 channels each) corresponding to the 64 channels of FEMs 7-12 are controlled by **asic042312** (side A). The masking/unmasking of the 16 channels of each ASIC chip is controlled by 4 hexadecimal digits where the leftmost hexadecimal digit controls channels 1-4, the second leftmost hexadecimal digit controls channels 4-8, the second rightmost hexadecimal digit controls channels 9-12,

Table 22: Linear fit (using points from figure 17) with slope and intercept for all channels in FEM10.

Channel	Slope	Intercept	Channel	Slope	Intercept
0	1910.15	2047.73	32	1907.95	484.432
1	1932.81	2039.15	33	1912.15	468.8
2	1903.11	2055.84	34	1905.97	471.508
3	1921.07	2047.68	35	1909.13	466.898
4	1924.11	2058.78	36	1897.44	484.172
5	1928.71	2044.73	37	1919.74	474.985
6	1926.21	2040.12	38	1911.81	480.229
7	1921.71	2039.9	39	1901.02	468.715
8	1911.36	2043.13	40	1913.23	479.639
9	1915.37	2046.41	41	1903.18	469.775
10	1914.45	2042.8	42	1918.84	473.04
11	1908.27	2049.98	43	1922.85	466.61
12	1915.15	2048.23	44	1911.67	479.292
13	1913.5	2053.87	45	1908.28	471.475
14	1906.46	2047.42	46	1912.61	471.64
15	1917.72	2045.04	47	1915.79	460.037
16	1906.33	2044.38	48	1895.57	482.093
17	1896.77	2046.67	49	1897.11	483.841
18	1900.71	2049.62	50	1899.4	488.571
19	1941.26	2043.68	51	1906.22	483.308
20	1931.81	2066.09	52	1903.04	482.815
21	1943.66	2051.21	53	1900.02	472.375
22	1932.54	2058.98	54	1897.16	488.307
23	1926.72	2043.49	55	1898.5	481.483
24	1931.97	2058.36	56	1908.88	482.655
25	1925.69	2044.82	57	1919.65	476.919
26	1942.43	2049.14	58	1908.75	486.644
27	1927.75	2046.1	59	1910.94	473.954
28	1919.11	2041.96	60	1913.04	478.895
29	1942.86	2045.91	61	1904.45	469.628
30	1934.58	2041.25	62	1907.6	485.088
31	1911.03	2060	63	1895.83	473.745

and the rightmost hexadecimal digit controls channels 13-16. The value of the hexadecimal digit can be understood by converting it into 4 binary digits with each binary digit controlling 1 of the 4 ASIC channels(masked is binary value 0 and unmasked is binary value 1). Two ASIC chips are controlled at a time using 8 hexadecimal digits with the leftmost 4 (abbreviated with a bold Italic capital \mathbf{L}) controlling one ASIC of the pair and the rightmost 4 (abbreviated with a

Table 23: Linear fit (using points from figure 17) with slope and intercept for all channels in FEM11.

Channel	Slope	Intercept	Channel	Slope	Intercept
0	1907.36	2040.92	32	1904.1	477.933
1	1893.71	2041.62	33	1915.31	482.358
2	1905.25	2045.96	34	1914.12	485.184
3	1910.79	2042.99	35	1913.47	477.123
4	1913.91	2043.87	36	1900.82	481.854
5	1910.29	2046.81	37	1910.08	470.335
6	1913.7	2046.62	38	1910.52	467.65
7	1913.66	2052.48	39	1920.18	477.831
8	1911.72	2049.39	40	1927.85	467.697
9	1913.17	2044.49	41	1917.47	468.023
10	1913.5	2042.27	42	1917.99	466.978
11	1908.33	2047.3	43	1914.72	472.178
12	1912	2038.27	44	1911.08	469.222
13	1913.2	2050.18	45	1908.04	470.726
14	1906.49	2049.68	46	1923.27	471.34
15	1907.71	2052.06	47	1907.05	481.649
16	1900.37	2051.64	48	1923.61	478.011
17	1918.35	2039.96	49	1923.2	473.945
18	1926.3	2041.6	50	1931.7	470.609
19	1913.39	2054.54	51	1910.61	477.391
20	1911.1	2042.5	52	1926.14	478.83
21	1945.94	2044.74	53	1926.03	476.211
22	1909.22	2047.22	54	1926.31	473.32
23	1925.6	2041.44	55	1922.82	481.713
24	1919.74	2041.69	56	1922.63	487.287
25	1911.82	2044.91	57	1919.99	471.777
26	1936.22	2044.49	58	1931.65	477.288
27	1919.11	2057.53	59	1928.49	474.972
28	1922.41	2045.49	60	1927.58	479.662
29	1921.97	2044.85	61	1916.82	476.611
30	1931.12	2050.62	62	1922.11	480.001
31	-	-	63	1910.21	490.031

bold Italic capital **R**) controlling the other ASIC of the pair. Figure 42 shows an example explaining the ASIC channel masking/unmasking option command for ASICs 6,8.

- The channels for ASIC chips 1 (**R**),3 (**L**) are controlled using the option **-0**. The channels for ASIC chips 4 (**R**),2 (**L**) are controlled using the option **-1**. The channels for ASIC chips 5 (**R**),7 (**L**) are controlled using the option

Table 24: Linear fit (using points from figure 17) with slope and intercept for all channels in FEM12.

Channel	Slope	Intercept	Channel	Slope	Intercept
0	1920.98	2042.43	32	1915.03	477.879
1	1912.48	2045.67	33	1911.32	485.933
2	1929.79	2053.09	34	1915.12	474.979
3	1919.07	2037.8	35	1917.55	491.515
4	1917.78	2046.26	36	1915.79	477.023
5	1937.65	2039.34	37	1919.25	490.232
6	1914.73	2039.15	38	1908.39	471.911
7	1894.5	2050.98	39	1894.33	486.247
8	1921.56	2049.2	40	1920.92	472.518
9	1919.55	2042.68	41	1906.75	479.799
10	1947.14	2058.16	42	1921.49	477.451
11	1952.72	2043.61	43	1921.1	471.666
12	1940.5	2047.83	44	1913.35	475.369
13	1914.04	2048.19	45	1909.65	473.058
14	1951	2050.03	46	1924.16	469.839
15	1921.58	2048.62	47	1916.74	472.377
16	1918.45	2051.15	48	1924.17	465.78
17	1910.15	2040.6	49	1920.68	476.029
18	1903.07	2060.54	50	1933.74	477.5
19	1941.63	2046.46	51	1942.45	470.285
20	1925.35	2056.37	52	1915.45	476.49
21	1930.16	2050.37	53	1927.31	477.356
22	1921.62	2048.22	54	1927.05	466.113
23	1896.32	2056.48	55	1939.19	474.433
24	1918.8	2053.68	56	1932.54	481.545
25	1945.34	2047.68	57	1928.15	473.092
26	1920.3	2053.52	58	1925.17	471.103
27	1943.65	2046.52	59	1931.34	470.543
28	1920.69	2047.26	60	1919.74	479.873
29	1938.09	2049.05	61	1922.23	478.656
30	1938.37	2045.69	62	1932.87	472.146
31	1924.62	2048.25	63	1925.14	482.531

- 2. The channels for ASIC chips 8 (**R**),6 (**L**) are controlled using the option
- 3. The channels for ASIC chips 9 (**R**),11 (**L**) are controlled using the option
- 4. The channels for ASIC chips 12 (**R**),10 (**L**) are controlled using the option
- 5. The channels for ASIC chips 13 (**R**),15 (**L**) are controlled using the option
- 6. The channels for ASIC chips 16 (**R**),14 (**L**) are controlled using the option
- 7. The channels for ASIC chips 17 (**R**),19 (**L**) are controlled using

Table 25: ASIC (1-48) to FEM channel (0-63) mapping.

ASIC #	FEM	FEM Channels	ASIC #	FEM	FEM Channels
1	7	32-47	25	1	0-15
2	7	16-31	26	1	48-63
3	7	48-63	27	1	16-31
4	7	0-15	28	1	32-47
5	8	32-47	29	2	0-15
6	8	16-31	30	2	48-63
7	8	48-63	31	2	16-31
8	8	0-15	32	2	32-47
9	9	32-47	33	3	0-15
10	9	16-31	34	3	48-63
11	9	48-63	35	3	16-31
12	9	0-15	36	3	32-47
13	10	32-47	37	4	0-15
14	10	16-31	38	4	48-63
15	10	48-63	39	4	16-31
16	10	0-15	40	4	32-47
17	11	32-47	41	5	32-47
18	11	16-31	42	5	16-31
19	11	48-63	43	5	48-63
20	11	0-15	44	5	0-15
21	12	32-47	45	6	0-15
22	12	16-31	46	6	48-63
23	12	48-63	47	6	16-31
24	12	0-15	48	6	32-47

the option **-8**. The channels for ASIC chips 20 (**R**),18 (**L**) are controlled using the option **-9**. The channels for ASIC chips 21 (**R**),23 (**L**) are controlled using the option **-a**. The channels for ASIC chips 24 (**R**),22 (**L**) are controlled using the option **-b**. For example, if the first channel out of 16 of all first 24 ASIC chips are to be unmasked with the rest of the channels masked, the command is: `./asic042312 -0 0x00010001 -1 0x00010001 -2 0x00010001 -3 0x00010001 -4 0x00010001 -5 0x00010001 -6 0x00010001 -7 0x00010001 -8 0x00010001 -9 0x00010001 -a 0x00010001 -b 0x00010001`.

The channels in the second 24 ASIC chips (16 channels each) corresponding to the 64 channels of FEMs 1-6 are controlled by **asic042312_secondset** (side B). The channels for ASIC chips 25 (**R**),27 (**L**) are controlled using the option **-0**. The channels for ASIC chips 28 (**R**),26 (**L**) are controlled using the option **-1**. The channels for ASIC chips 29 (**R**),31 (**L**) are controlled using the option **-2**. The channels for ASIC chips 32 (**R**),30 (**L**) are controlled using the option **-3**. The channels for ASIC chips 33 (**R**),35 (**L**) are controlled using the option

- 4. The channels for ASIC chips 36 (**R**),34 (**L**) are controlled using the option
- 5. The channels for ASIC chips 37 (**R**),39 (**L**) are controlled using the option
- 6. The channels for ASIC chips 40 (**R**),38 (**L**) are controlled using the option
- 7. The channels for ASIC chips 41 (**R**),43 (**L**) are controlled using the option
- 8. The channels for ASIC chips 44 (**R**),42 (**L**) are controlled using the option
- 9. The channels for ASIC chips 45 (**R**),47 (**L**) are controlled using the option
- a. The channels for ASIC chips 48 (**R**),46 (**L**) are controlled using the option
- b. For example, if all of the channels of ASIC chips 39,40 of the second 24 ASIC chips are to be unmasked with the rest of the channels masked, the command is:
`./asic042312_secondset -0 0x00000000 -1 0x00000000 -2 0x00000000 -3 0x00000000 -4 0x00000000 -5 0x00000000 -6 0xffff0000 -7 0x0000ffff -8 0x00000000 -9 0x00000000 -a 0x00000000 -b 0x00000000.`

Additionally, the ASIC preamplifier gain can be set at 4 predetermined settings. The option **-g** is used to adjust the gain setting for both **asic042312** and **asic042312_secondset**. There are four values (**0,1,2,3**) for the option **-g**. **0** (default setting/no **-g** option input) has a gain setting 4.7 mV/fC. **1** has a gain setting 7.8 mV/fC. **2** has a gain setting 14 mV/fC. **3** has a gain setting 25 mV/fC. For example, if all of the first set of ASIC channels is to be run with gain setting 14 mV/fC, the following command is used: **asic042312 -v -g 2**.

Additionally, the ASICS have different peaking time configurations at 4 predetermined settings. The option **-p** is used to adjust the peaking time setting for both **asic042312** and **asic042312_secondset**. There are four values (**0,1,2,3**) for the option **-p**. **0** has a peaking time setting of 0.5 μ s. **1** has a peaking time setting of 1 μ s. **2** (default setting/no **-p** option input) has a peaking time setting of 2 μ s. **3** has a peaking time setting 3 μ s. For example, if all of the second set of ASIC channels is to be run with peaking time setting of 3 μ s, the following command is used: **asic042312_secondset -v -p 3**.

All of the options for the ASIC configurations can be seen by typing the command: **./asic042312 -help** (or **./asic042312_secondset -help**).

To mask all the bad ASIC channels in Table 26 while keeping all the good ASIC channels unmasked, the following two masking commands are used:

- `./asic042312 -0 0xffff7fff -1 0xffffffff -2 0xffffffff -3 0x7fffffff -4 0xffff7fff -5 0xbfffffff -6 0xffffffff -7 0xffffffff -8 0xffffffff -9 0x7fffffff -a 0xffffffff -b 0xffffffff`
- `./asic042312_secondset -0 0xefffffff -1 0xffffdfff -2 0xffffffff -3 0x7fff7fff -4 0xffffffff -5 0x7fff7fff -6 0xffffffff -7 0xffffffff -8 0xffffffff -9 0xffffffff -a 0x7f7f7fff -b 0x7fff7fff`

11 Appendix E: Bad ASIC Channels

By looking at the signals when the ASICS are completely unmasked with an input pulse voltage of 500 mV, the bad ASIC channels (ASIC channels that do not change ADC values from baseline in response to input pulse voltage) for the 12 FEMs can be identified. This was done using the crate readout (slow

controller readout) and the results are tabulated in Table 26. The results for the bad ASIC channels remain the same for the XMIT readout (fast readout). The bad ASIC channels does not change for different input pulse voltage. A test to determine if the bad ASIC channels for slow controller readout was constant and consistent was done at the input pulse voltage of 500 mV and the results showed that the bad ASIC channels remained the same.

Table 26: Bad ASIC channels for the 12 FEMs. The 64 channels for each FEM are numbered from 0-63. Done using the crate readout. Same with XMIT readout.

FEM Number	Bad Channels
1	28,45
2	47,63
3	47,63
6	15,23,31,47,63
7	47
8	31
9	30,47
11	31

12 Appendix F: Calibration Run Readout Settings

13 Data decoding

13.1 Slow readout

Figure 43 shows a printout of the slow controller data readout in uncompressed text file format. The data starts with a set of 5 header words in a single row consisting of information for a single event for a single FEM. The next row consists of a single word whose value is the total number of 32-bit ADC data or channel header words in the event for a single FEM. The data is in 32-bit hexadecimal format arranged from left to right and then top to bottom in 9 columns. The leftmost column counts the total number of 32-bit data words up to that point. The other 8 32-bit words contain ADC data (or channel header data). Each 32-bit word consists of two 16-bit word with the rightmost 16-bit word being the first of the two words and the leftmost 16-bit word being the second of the two words. There are two types of words: 16-bit ADC value words and 16-bit channel header words. Each ADC value 16-bit word consists of a 0 followed by three hexadecimal digits corresponding to a maximum of 4096 different ADC values (12-bit ADC). Each 16-bit channel header signifies a new channel begin (4XXX) or channel end (5XXX) where XXX gives the channel

number in hexadecimal within each FEM (0-63). After all the data for the 64 channels for a single event of a single FEM is outputted, the format repeats itself for the event for the next FEM. After all the data for the event is outputted, the format repeats itself for the next event until all events are outputted.

13.2 XMIT readout

Figure 44 shows a printout of the XMIT data readout in uncompressed text file format. The data is in hexadecimal format arranged from left to right and then top to bottom in 8 32-bit word columns which contain ADC data. The data starts with **ffffffff** which signifies the beginning of an event for all the channels for all the FEMs. 5 32-bit header words are next consisting of information of each FEM. The 32-bit data ADC words come next. Each 32-bit word consists of two 16-bit word with the rightmost 16-bit word being the first of the two words and the leftmost 16-bit word being the second of the two words. There are two types of words: 16-bit ADC value words and 16-bit channel header words. Each ADC value 16-bit word consists of a 0 followed by three hexadecimal digits corresponding to a maximum of 4096 different ADC values (12-bit ADC). Each 16-bit channel header signifies a new channel begin (4XXX) or channel end (5XXX) where XXX gives the channel number in hexadecimal within each FEM (0-63). After the last channel end (503f) of the FEM comes the 5 32-bit header words of the new FEM before the new channel begin (4000) of the new FEM. After all the data for the event is outputted, the data ends with **e0000000** which signifies the end of an event for all the channels for all the FEMs. The format repeats itself for the next event until all events are outputted.

14 Appendix G: Board Positions and Serial Numbers

Table 27: Board positions (along with serial numbers) in the crate.

Board Type	Position	Serial Numbers	
Trigger Board	Slot 2	E26878	
Xmit Board	Slot 6	E33865	
FEM P2 Board	Slot 7	BNL PAT0022	Nevis E43477
FEM P1 Board	Slot 8	BNL PAT0026	Nevis E43464
FEM P12 Board	Slot 9	BNL PAT0025	Nevis E43472
FEM P3 Board	Slot 10	BNL PAT0019	Nevis E43471
FEM P4 Board	Slot 11	BNL PAT0017	Nevis E43479
FEM P5 Board	Slot 12	BNL PAT0028	Nevis E43466
FEM P6 Board	Slot 13	BNL PAT0030	Nevis E43469
FEM P7 Board	Slot 14	BNL PAT0018	Nevis E43465
FEM P8 Board	Slot 15	BNL PAT0020	Nevis E43474
FEM no # Board	Slot 16	BNL PAT0024	Nevis E43470
FEM P10 Board	Slot 17	BNL PAT0021	Nevis E43467
FEM P11 Board	Slot 18	BNL PAT0029	Nevis E43468
Controller Board	Slot 20	4004568A00 11030003	
Back Plane Board	Back Plane	4004552A00 11050003	
Clock Attached to Back Plane	Back Plane	4004567A00 11030004	

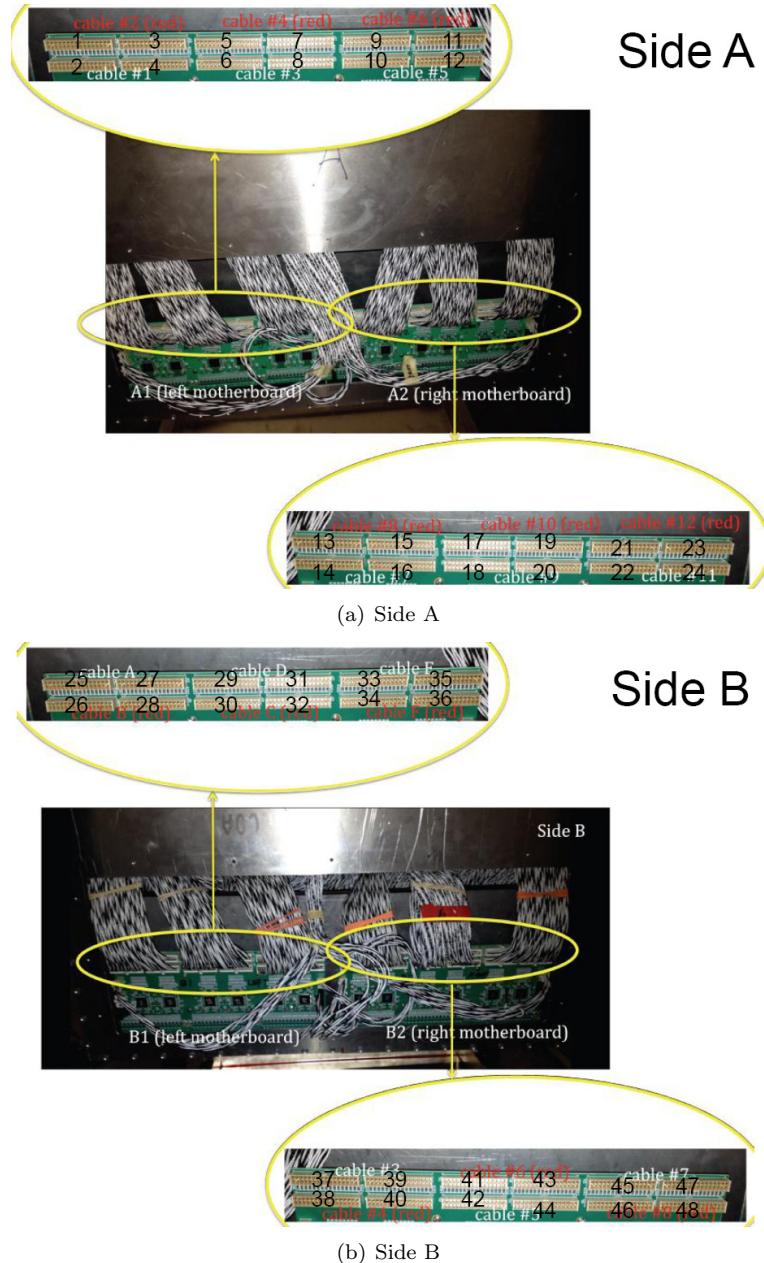


Figure 41: The physical setup of the ASIC motherboards in the test stand. Note the numbering on the ASIC cable slots, which is used to identify the individual ASICs in this document.

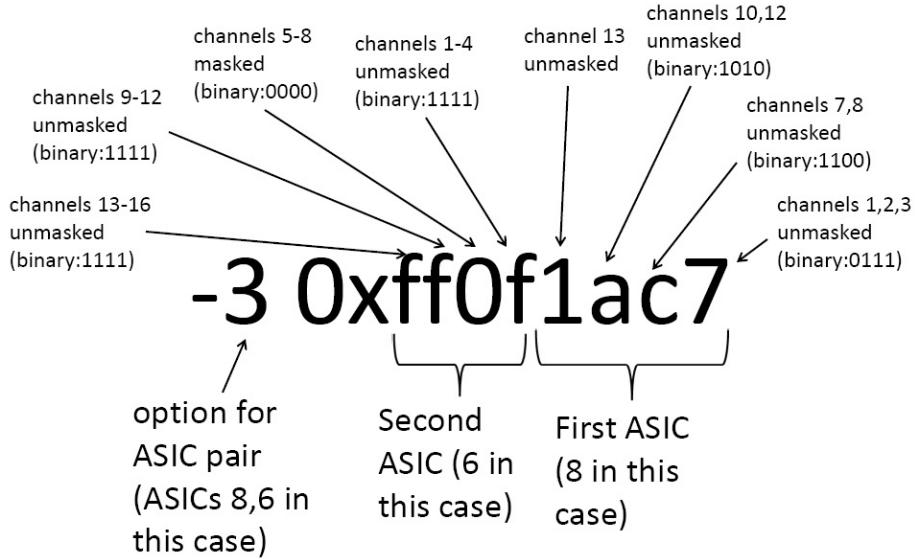


Figure 42: An example explaining the ASIC channel masking/unmasking option commands. In this case, channels 1-3,7-8,10,12-13 in ASIC 8 are unmasked and channels 1-4,9-16 in ASIC 6 are unmasked. All other channels in ASIC 6,8 are masked.

```

f227ffff, fdffff001, f001f000, f055f000, f33cfb79
3840
 0 7fe4000 80007ff 8010800 7fe07ff 7ff07ff 8010801 8010801 8010802
 8 7fc07ff 80107fd 7ff0801 8030801 7ff0801 7ff07fe 80007ff 8000800
16 8020801 7ff0801 8020800 7ff0802 7fd07fd 80007fe 87c0802 bb70b26
24 89009f7 806081a 7fd07ff 7ff07fe 8040800 8030805 8020800 8010803
32 8010801 7ff0800 8000800 80107fe 8010802 8030802 7fc07ff 7ff07fd
40 80207fe 8000802 8000801 80107ff 7ff0801 8030801 7ff0803 80107ff
48 8000802 8040803 7fe0800 80007ff 7ff0800 80007fe 8010800 7fe0802
56 80107fe 7ff0800 8020800 50000801 8014001 7fe07fe 7fd07fd 7fd07fe
64 7fe07ff 80107fe 8000801 8000801 7fe07fe 7fc07fd 7fe07fd 7fa07fc
72 7fe07fb 7fd07fe 7fe07fc 80007ff 7ff07ff 7ff0800 7fb07fd 7ff07fe
80 7fc07fc 7fd07fe 87c07fd bb60b2c 88d09ef 7ff0819 7fb07f9 80007fe
88 8030801 7fd07ff 8010800 7fc0800 7ff07ff 7fe07fe 7fe07ff 7fa07fd
96 7fe07f9 8010801 8010801 7fa07ff 7fb07f9 80007fe 80107fe 7ff0802
104 7ff07fd 7fc07fd 7fe07ff 7ff07fc 80007fd 7ff0802 7fd07fe 7ff07fd
112 8020803 7fa07fe 7fe07fc 7fc07fd 7fd07fb 8000803 7fb07fc 50010800
...

```

Figure 43: Readout raw ADC values in hexadecimal for the first two events in slow controller readout. The header words are top are in blue. The total number of 32-bit ADC data or channel header words in the next line is in orange. The counter for the 32-bit data words up to that point are in the leftmost column is in purple. The start of an event for one channel of one FEM is in green. The end of an event for one channel of one FEM is in red. The data ADC values are in black.

```

ffffffffff file7ffff fdffff001 f001f000 f043f000 f47efb7a 7fe4000 80107ff
8010802 7ff07ff 7fd0800 80107fc 8000804 7ff07fd 8010802 7ff07fe
8010800 8010800 7ff0800 80207ff 8000803 8040800 7ff0803 80107fe
8010802 8020800 80007fe 7ff0800 81407ff bf00a24 8f90ab3 8090835
8010802 8000800 80207ff 8050805 7ff0800 8010803 7ff07ff 7ff07ff
8010800 8020800 8000802 8040801 8040805 7fd07ff 80007fe 8020800
8000802 80007ff 8000801 8020801 8010803 8010802 7ff0801
8010800 8020803 8010801 8010801 7ff0802 7ff07fd 8020803 8060801
8010803 500007fe 7fd4001 8010801 80107fe 7ff0801 7fc07fd 7fb07fc
7fe07fc 80207ff 7ff0800 7fe0800 7fd07fd 8030800 7fd0801 7fb07fb
7fd07fc 8030800 7fc07ff 7fe07fd 7fd07fd 7fd07fe 7fe07fe 7fd07fb
8120800 bed0a24 8f20aab 8090830 8000803 80007fe 8010801 7fe0801
7fd07fc 7ff0800 8020803 8000800 7fb07fe 7ff07fe 8020801 7ff0800
80107fe 7fd07fe 8000800 7fd07fd 8000800 7ff07fc 8010800 7ff0803
7fb07fd 7fe07fa 7fe0801 7fe07fd 80007ff 7fe07ff 7ff0800 80207fe
7ff0802 7fd07fd 80107ff 7ff07ff 7fe07fe 500107fe ... 1e001e0
1e001e0 1e801e4 1e301e6 1e101df 503f01e3 e0000000

```

Figure 44: Readout raw ADC values in hexadecimal for the first two events in XMIT readout.