Micro-BooNE LArTPC FPGA Processing

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Fermilab
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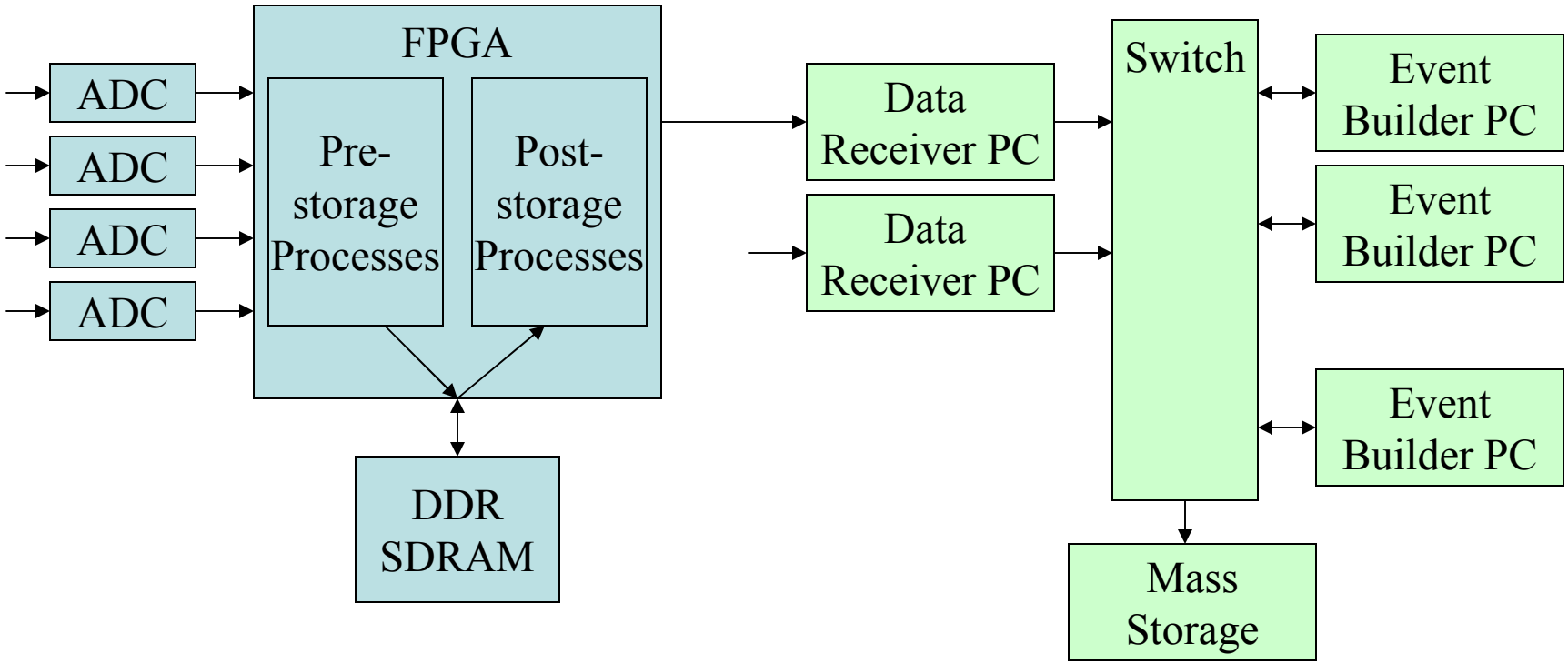
Pre-Introduction

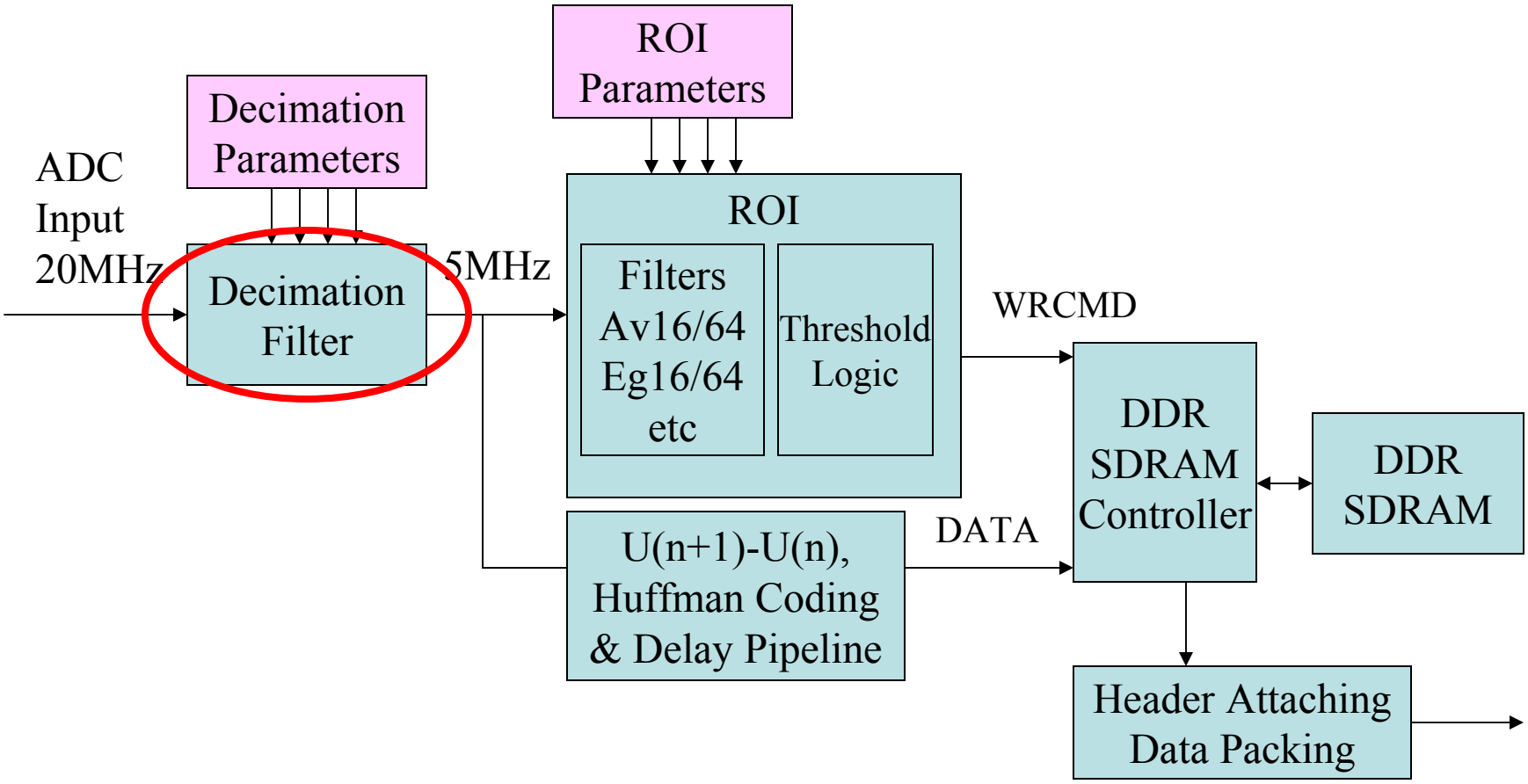
- Do not give Chen a hard time. Save your questions for Wu after he comes back ☺
- High volume of the raw data can be simply compressed without information loss in FPGA and/or PC.
- DC operation, i.e., collecting all data, with good compression is not totally impossible.
- Again, do not give Chen a hard time ☺

Introduction

- All processes in FPGA can be **lossless** only.
- All data **deletions** can be deferred to PCs.
- FPGA may also calculate data deleting ***suggestions*** for PCs to improve process speed in PCs.

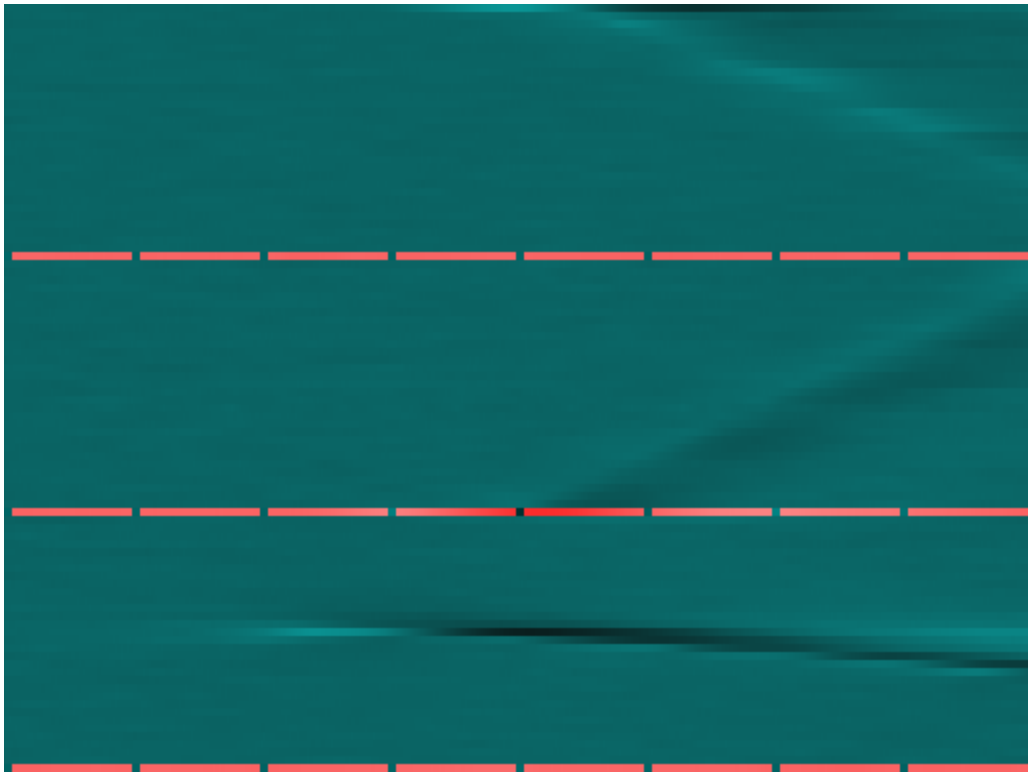


Details in FPGA

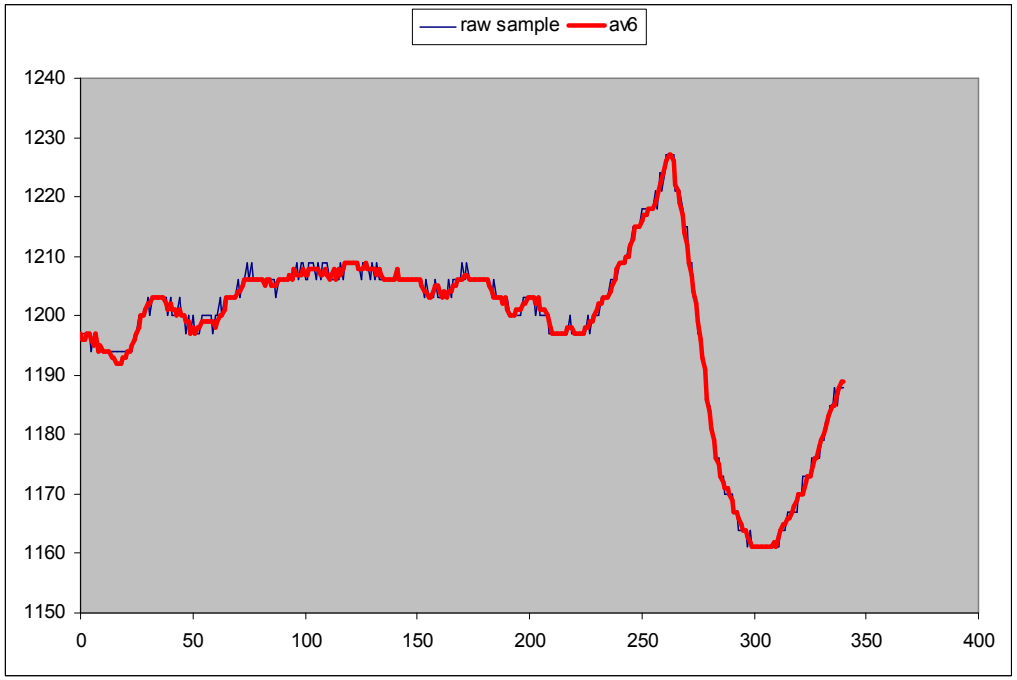


- The process time is O(n), i.e., no large buffers are needed in FPGA.
- Processes parameters are programmable.

30MHz Event Display: R156_E101

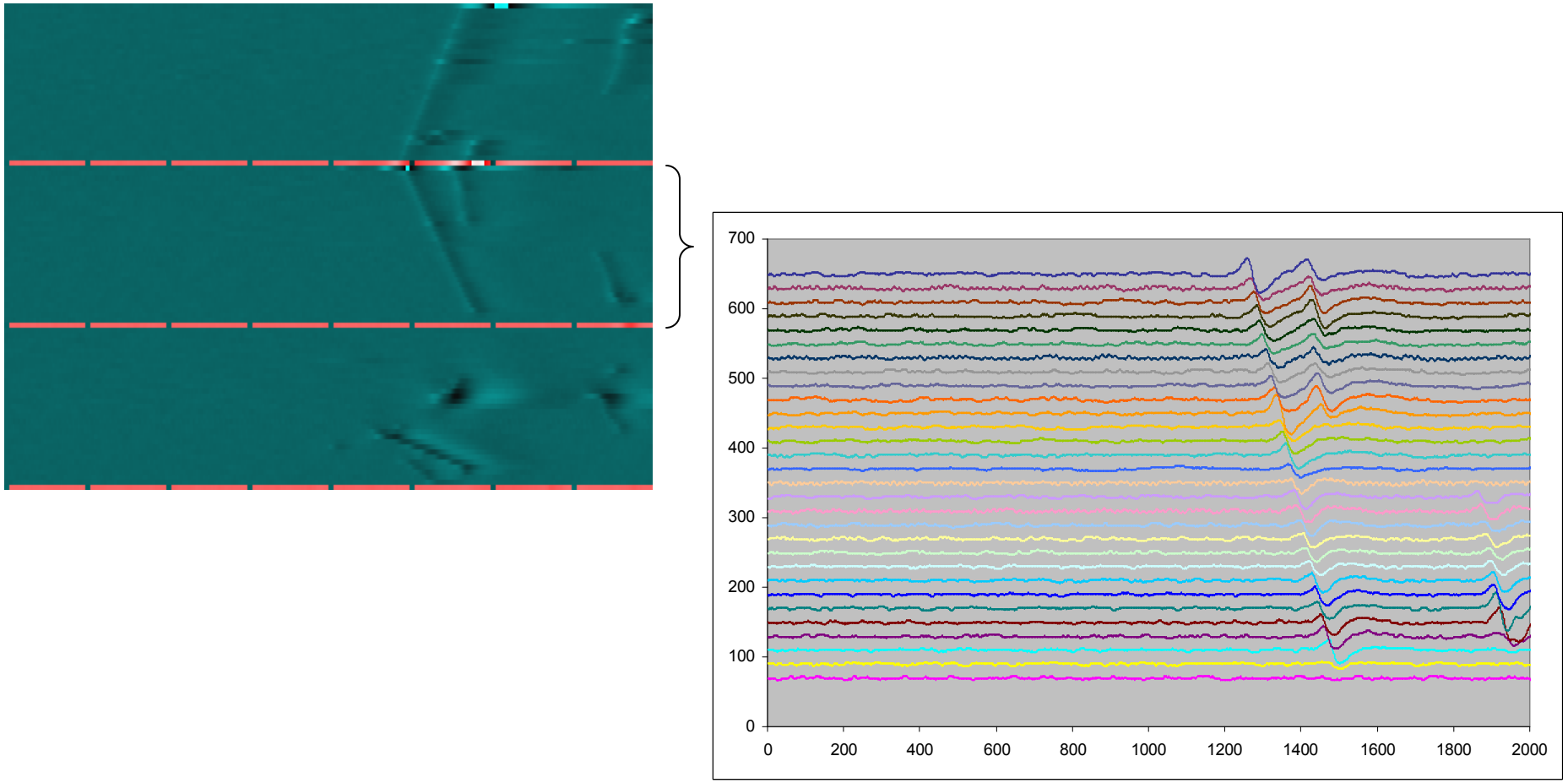


The 30MHz Data: *-30MHz/6*

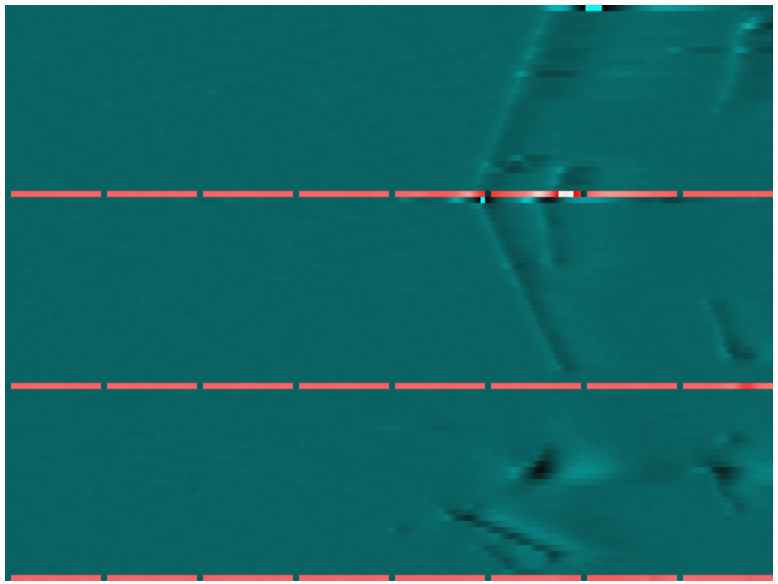


- Raw Sample: 1 out of 6.
- Av6: average of 6.
- Averaging reduces high frequency noise but not low frequency noise.
- The implementation cost is very low.
- The decimation filtering is considered a “standard” procedure. It provides additional safe guard for robust performance in case noise level becomes high.

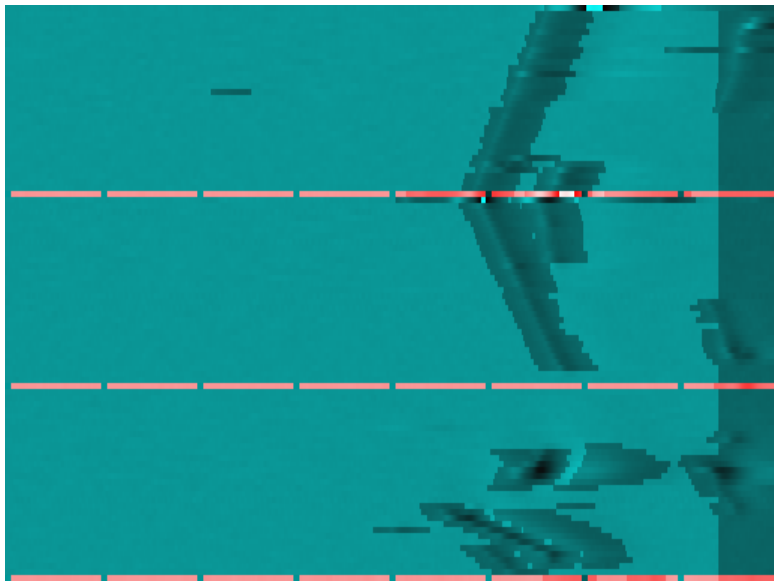
5 MHz Raw Data, R089_E175, W33-62



5MHz Event Display: R089_E175

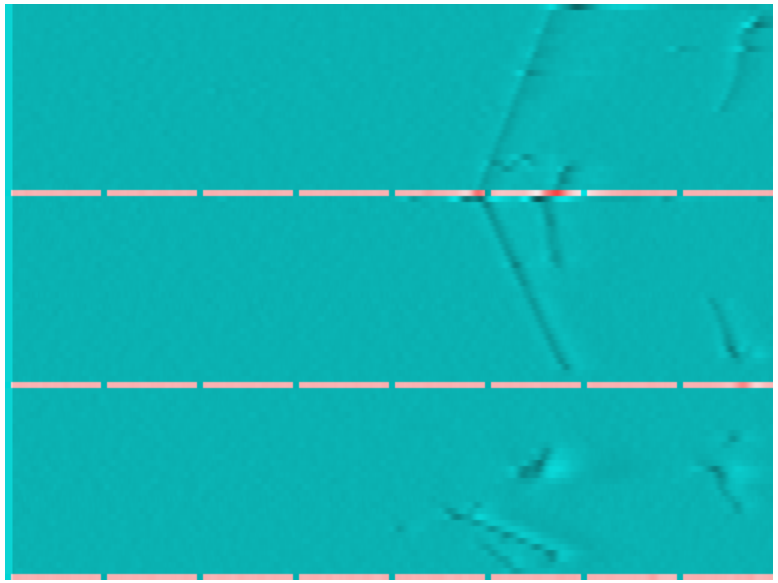


Raw
Data



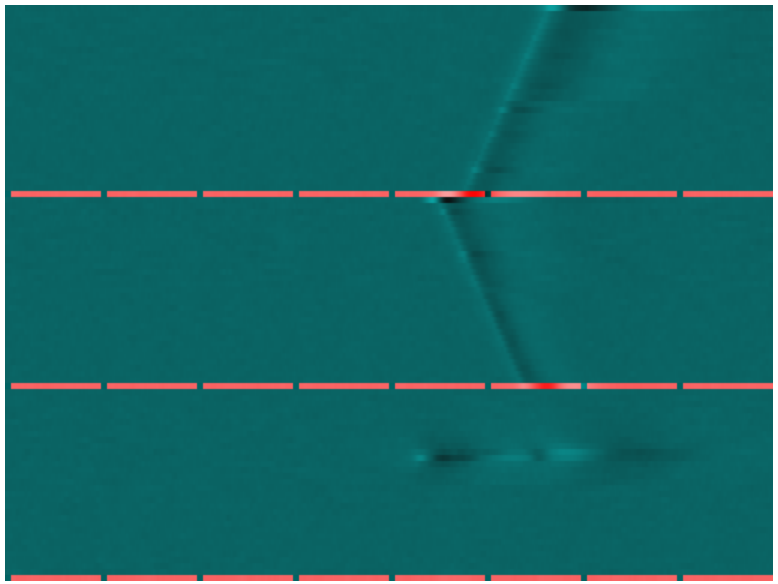
"ROI" marking,
|U(n+70)-U(n)|>10 (n to n+100)
This is only an attempt.

U(n) is the nth ADC value

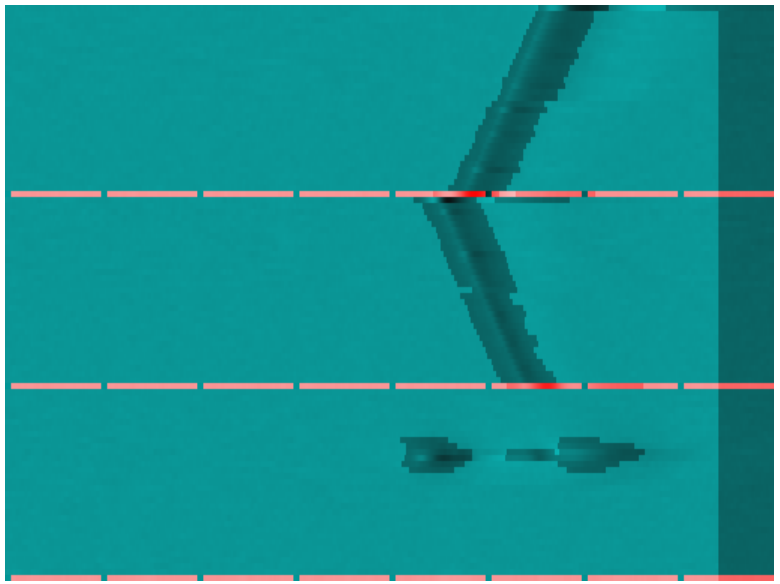


"Track finding"
U(n)-U(n-20)
This is only an attempt.

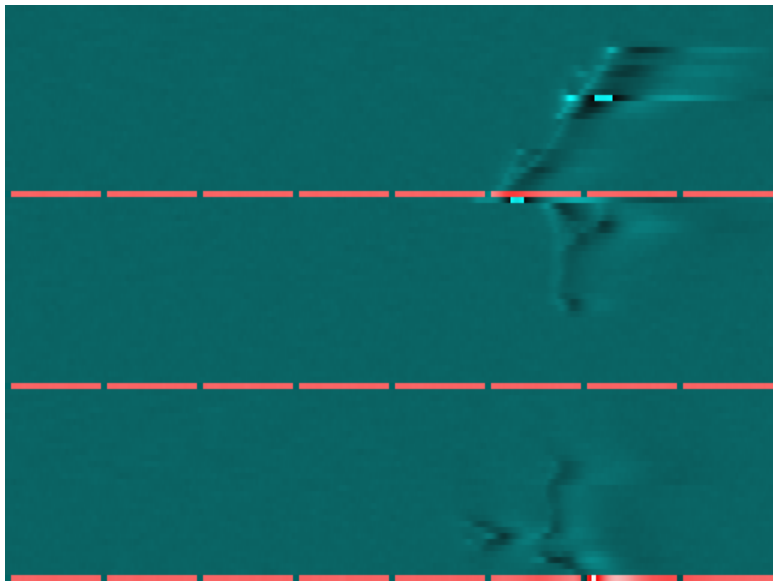
5MHz Event Display: R089_E104



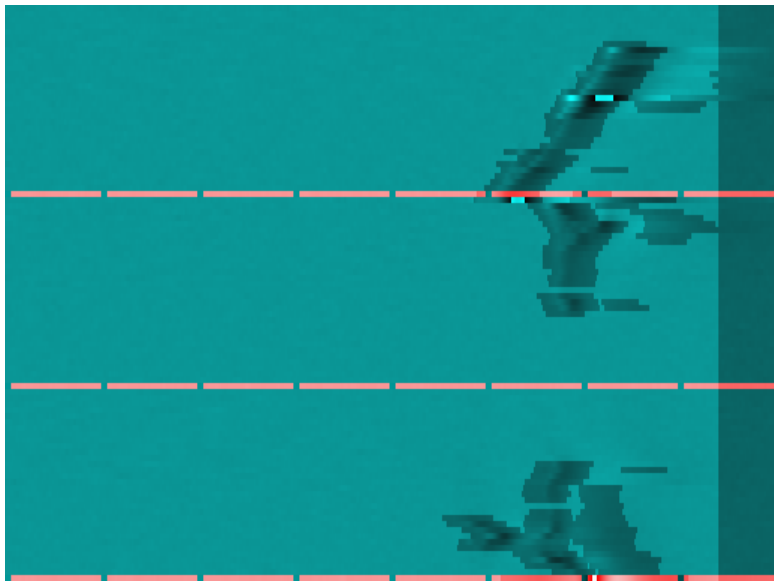
Raw
Data

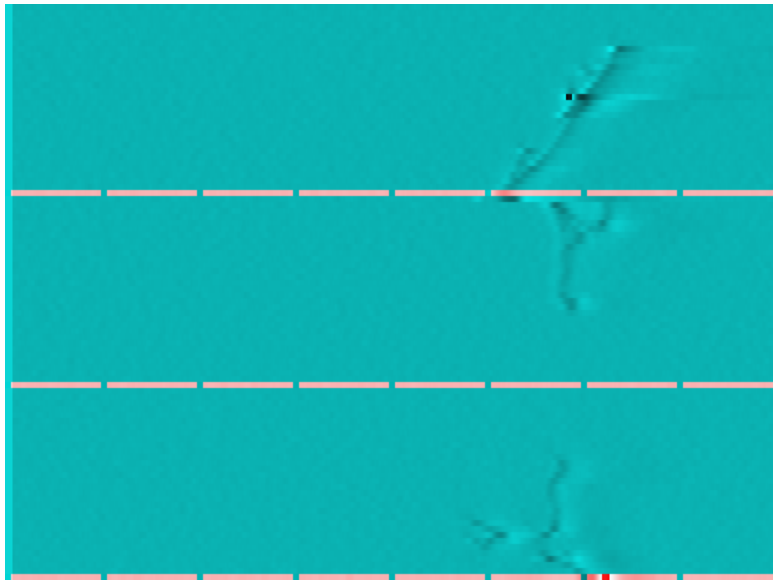


5MHz Event Display: R097_E115

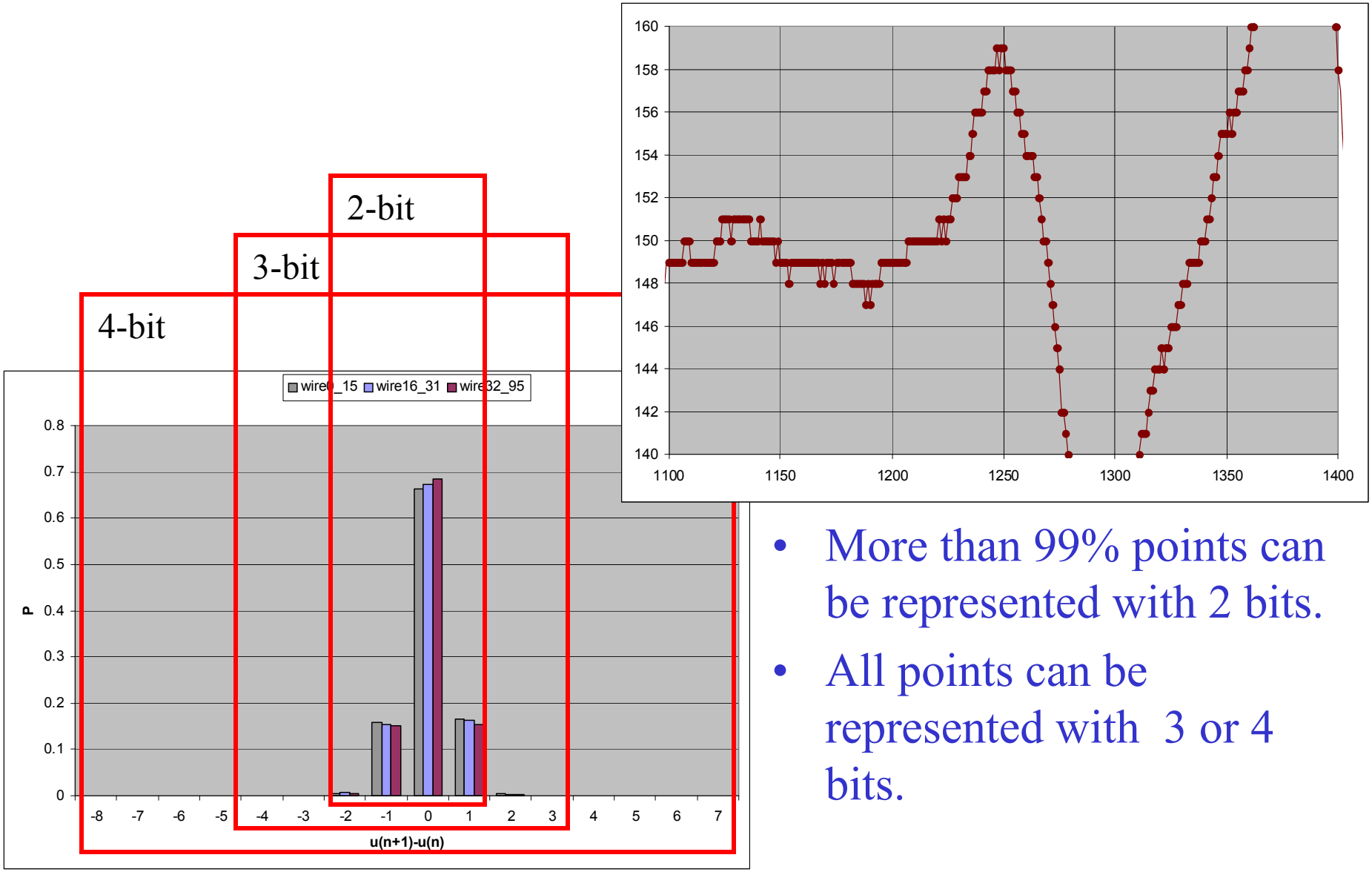


Raw
Data



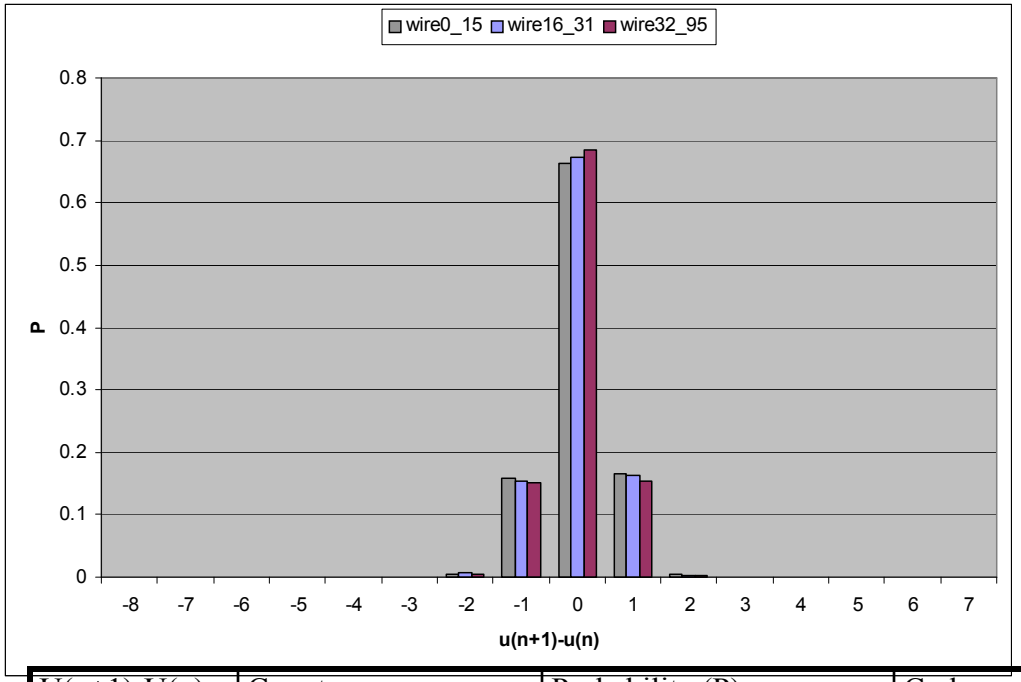


Slow Variation of Raw Data



- More than 99% points can be represented with 2 bits.
- All points can be represented with 3 or 4 bits.

Huffman Coding (A Lossless Compressing)



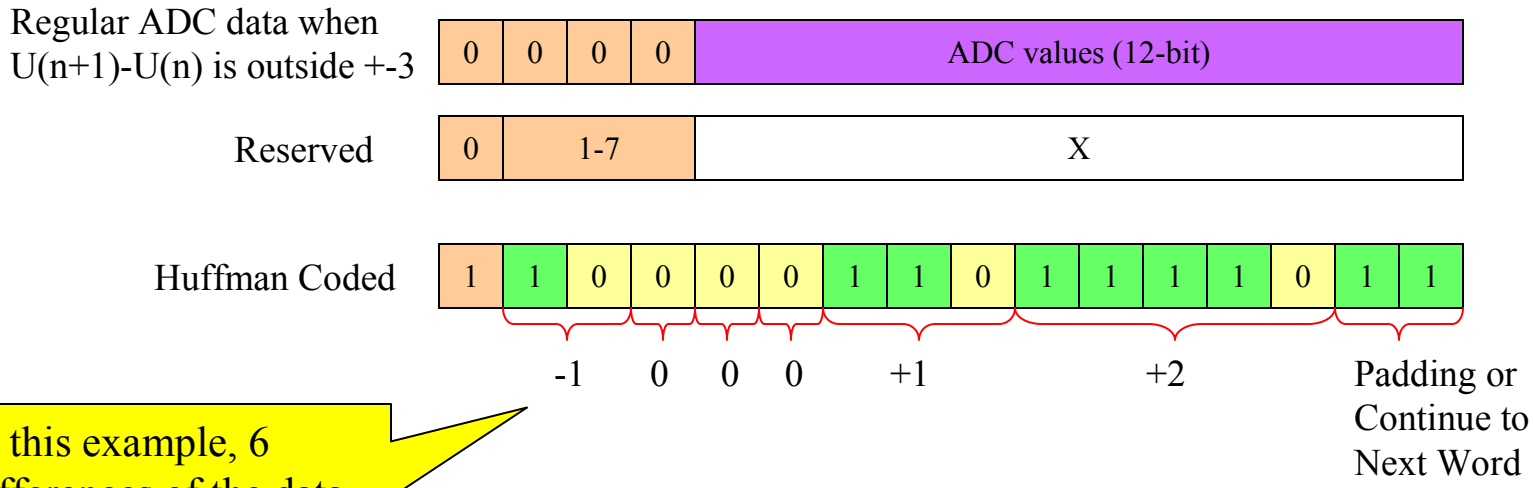
- Shorter codes (1-7 bits) are assigned to differences with higher probability (in our case -3 to +3).
- Any differences outside +-3 use 16 bits.
- In this example, coding rate is 1.53 bits/sample.
- In other events, coding rate is also ~1.5 bits/sample.

U(n+1)-U(n)	Count	Probability (P)	Code	No. of bits (N)	P*N
-4 and others	11	0.000179124	Full 16 bits word	16	0.002866
-3	45	0.00073278	111110	6	0.004396
-2	358	0.005829669	1110	4	0.023318
-1	9681	0.157645335	10	2	0.315290
0	40867	0.665477935	0	1	0.665477
+1	10145	0.165201107	110	3	0.495603
+2	298	0.00485263	11110	5	0.024263
+3	5	8.142E-05	1111110	7	0.000569
total		1.00			1.53

Data Words with Huffman Coding

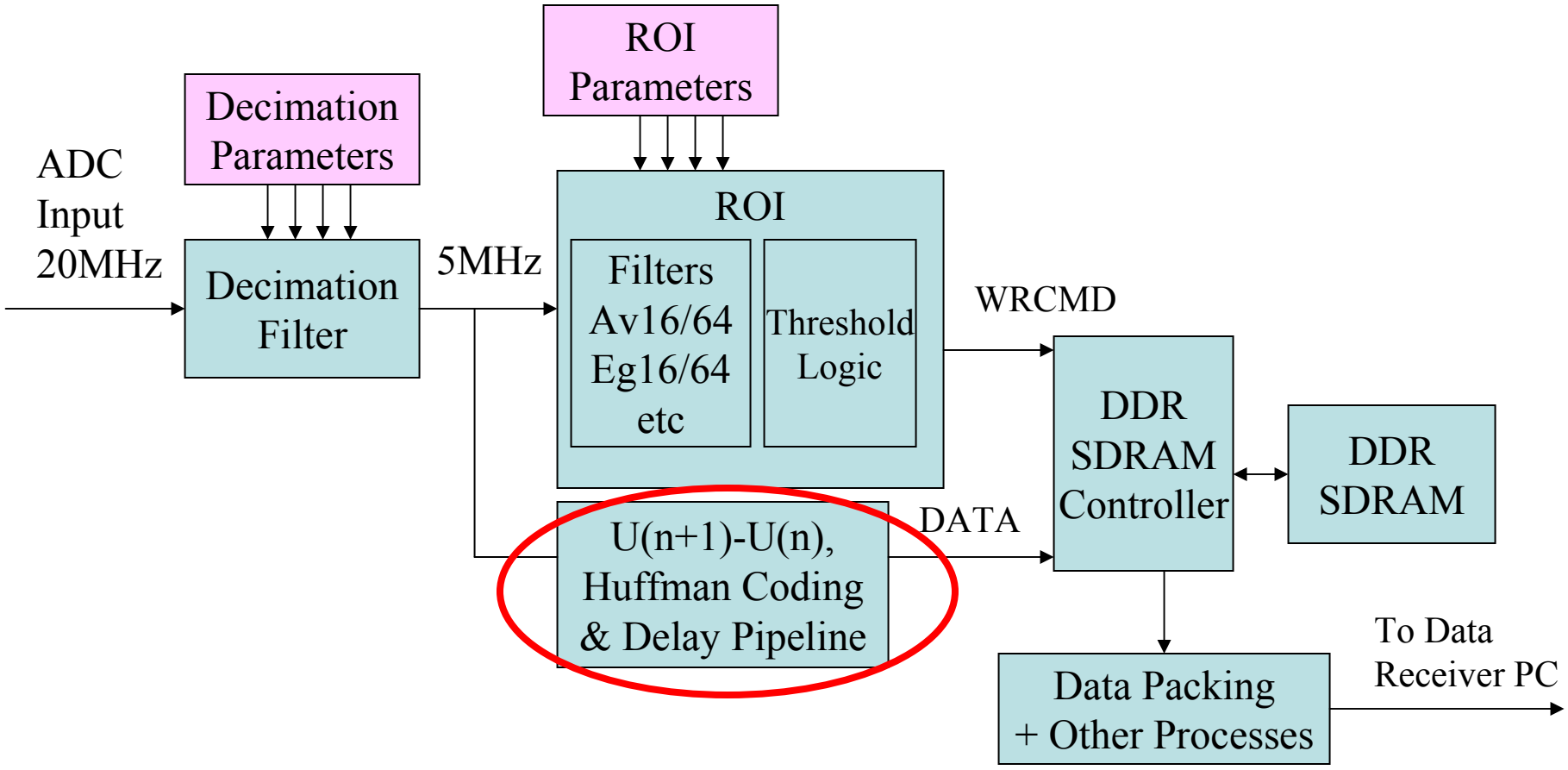
U(n+1)-U(n)	Code
-4 and others	Full 16 bits word
-3	111110
-2	1110
-1	10
0	0
+1	110
+2	11110
+3	1111110

- Huffman codes are self-punctuated, i.e., a 0 is always the code end.
- We pack the Huffman codes into 16-bit data words for additional fault recovery ability at the cost of reduced compression efficiency.



In this example, 6 differences of the data samples are packed in the 16-bit data word.

Details in FPGA



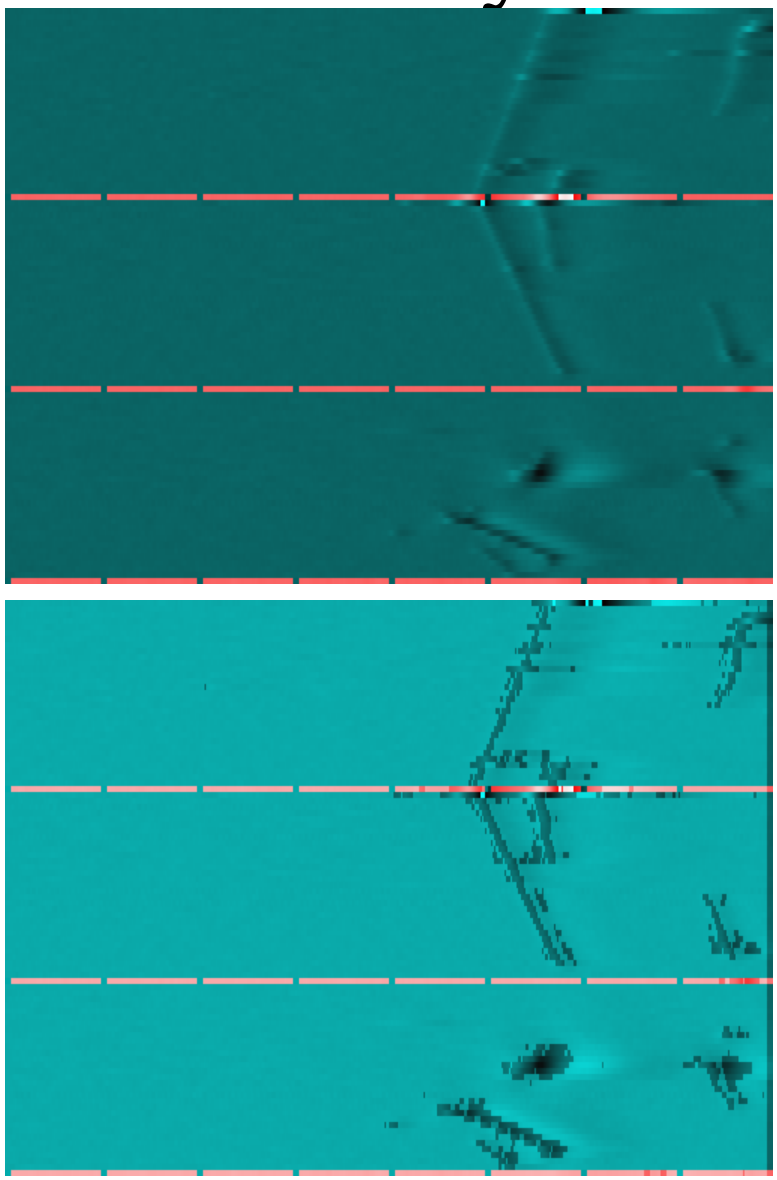
- The process time is O(n), i.e., no large buffers are needed in FPGA.
- Processes parameters are programmable.

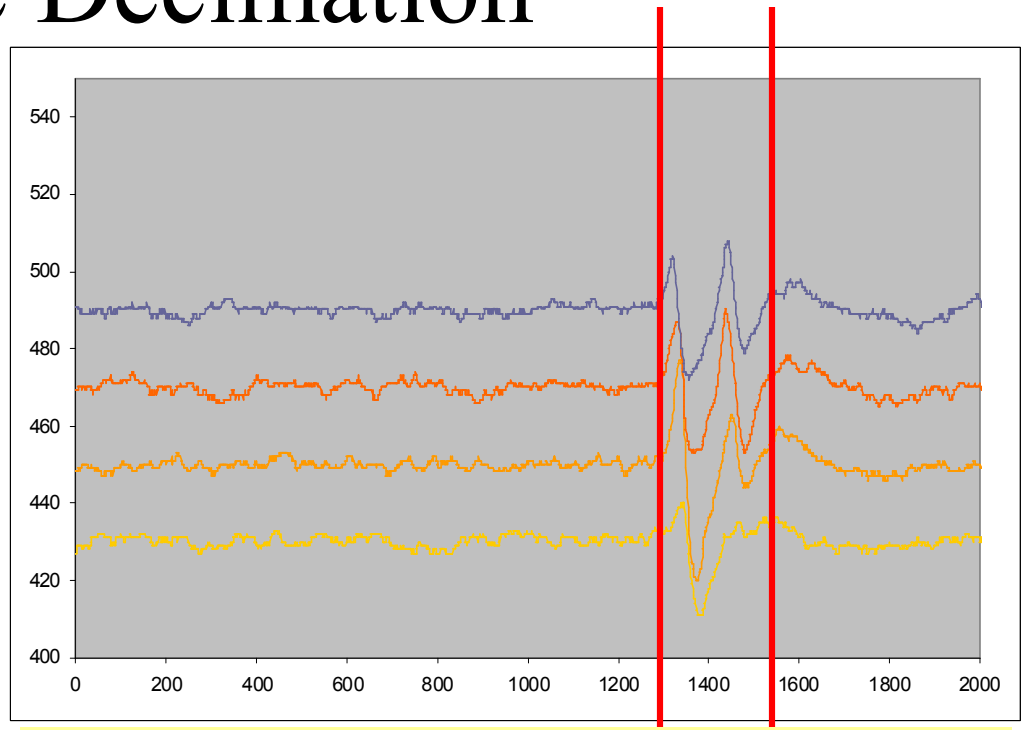
Data Rate for Storage in TPC Readout Board

Storage Mode & Rate	Transfers with 64-bit SDRAM for 64 channels (400 M Transfers/s max)	Storage Capacity 256 MB	Data Rate to PC (/Board)
Chronicle 5 MHz	80 M Transfers/s	0.4 sec	5.12Gbits/s
Huffman Coding 4bits/sample, 5 MHz	Peak: 80 M Transfers/s Average: 20 M Transfers/s	1.6 sec	1.28Gbits/s

- One RJ-45 connector: 4pairs x 320Mb/s/pair = 1.28Gb/s.
- Four RJ-45 connectors: 5.12Gb/s.
- The data rate for the links to operate is intended to be as low as possible.
- Assume 4bits/sample for Huffman Coding to be conservative.

Dynamic Decimation



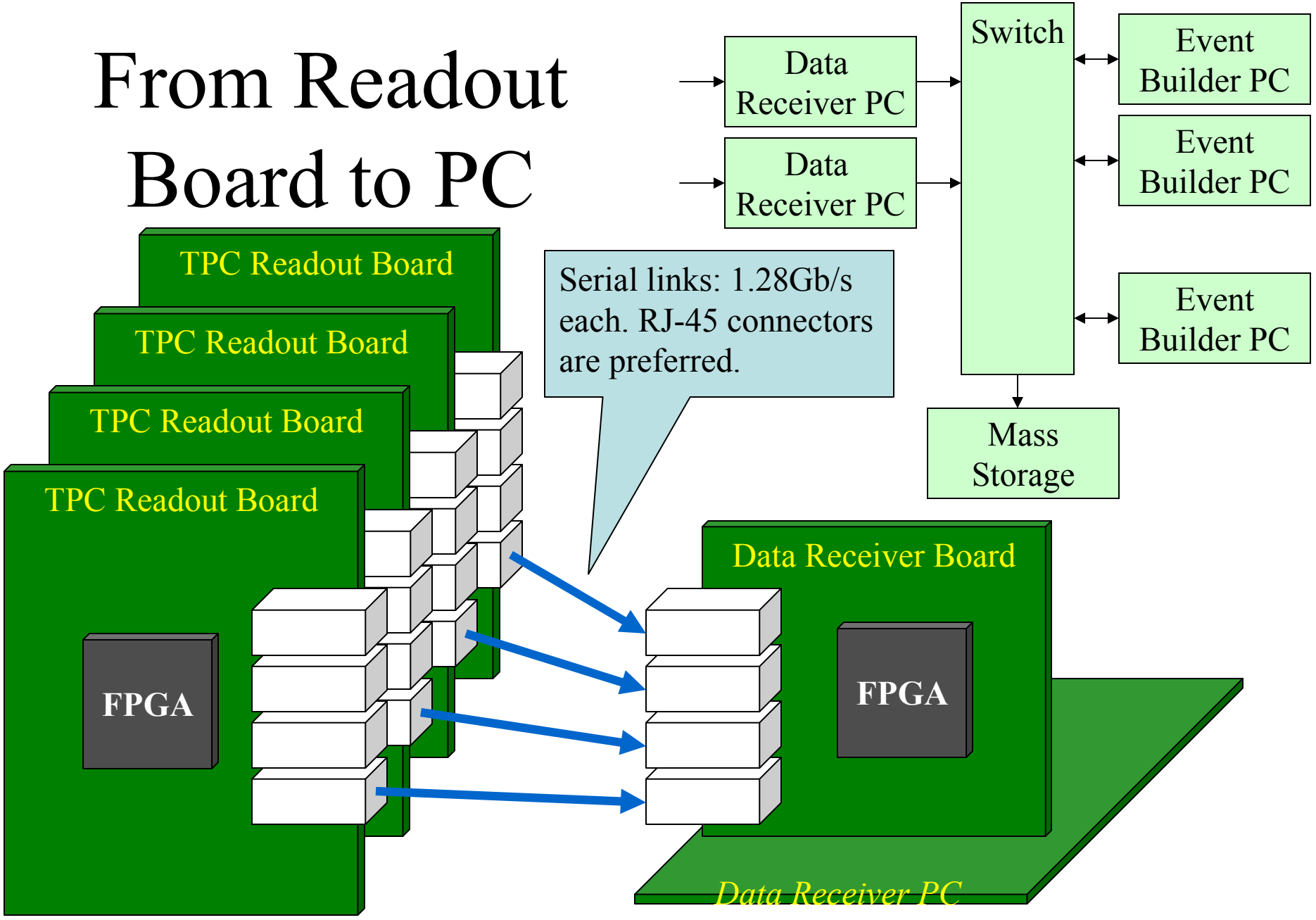


- Only small time intervals must be sampled at 5MHz.
- Most time intervals can be sampled with lower frequency, e.g., (5/16)MHz without losing useful information. (These wire*time areas are marked with lighter color in the lower left picture).

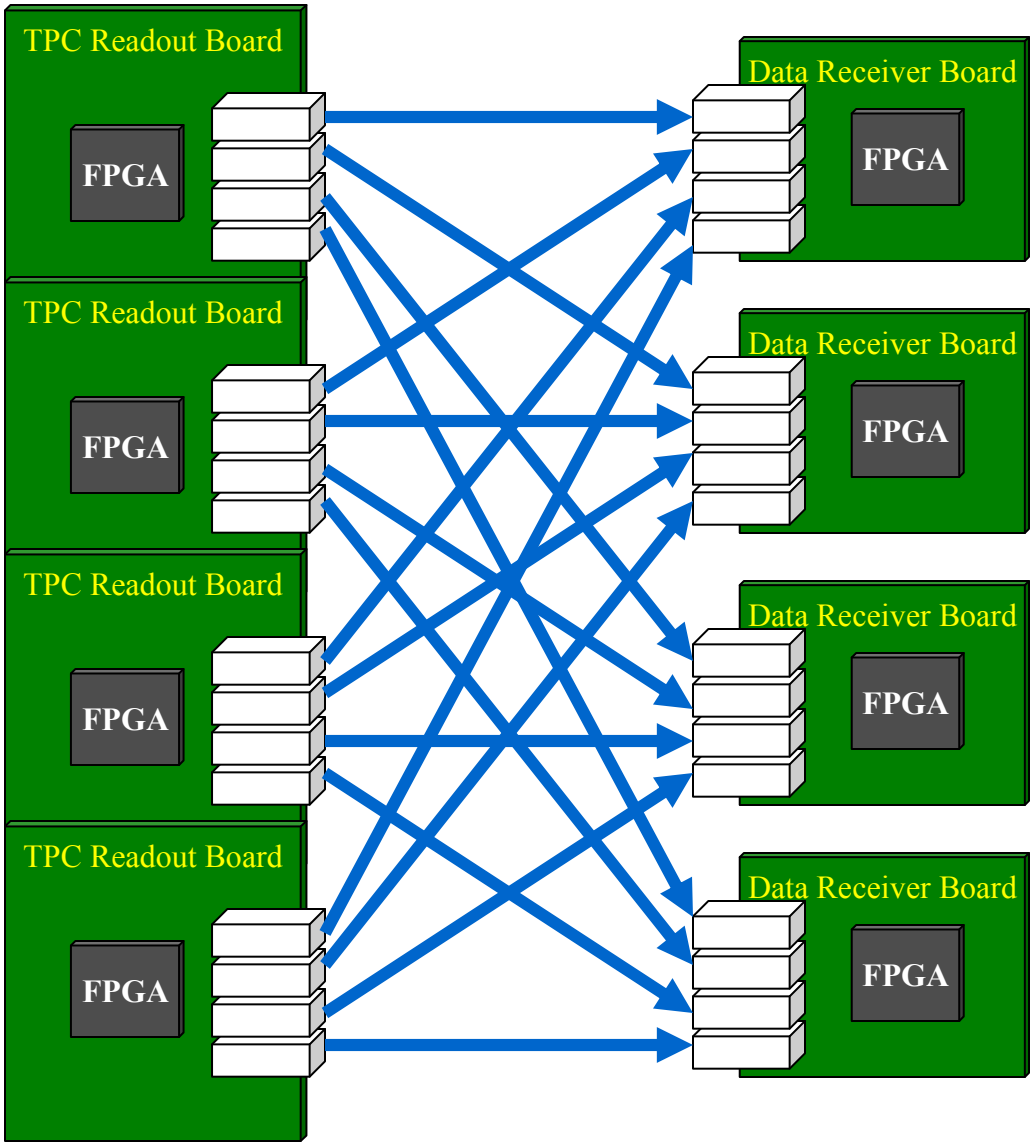
Remarks on Dynamic Decimation

- Dynamic decimation is not lossless strictly speaking. But the raw data loss is only in the region with no significant change of the raw data. In this region the inputs are still sampled, but at a much lower frequency.
- Another factor of 10 or so data reduction is anticipated but it is to be studied.
- Low frequency variations, such as temperature drift, 60Hz AC noise etc. can still be tracked.
- The process can be done in FPGA but it can also be done in PC. Another possibility is to **tag** the excessive data in FPGA and to **delete** in PC.
- Again, do not give Chen a hard time ☺

From Readout Board to PC



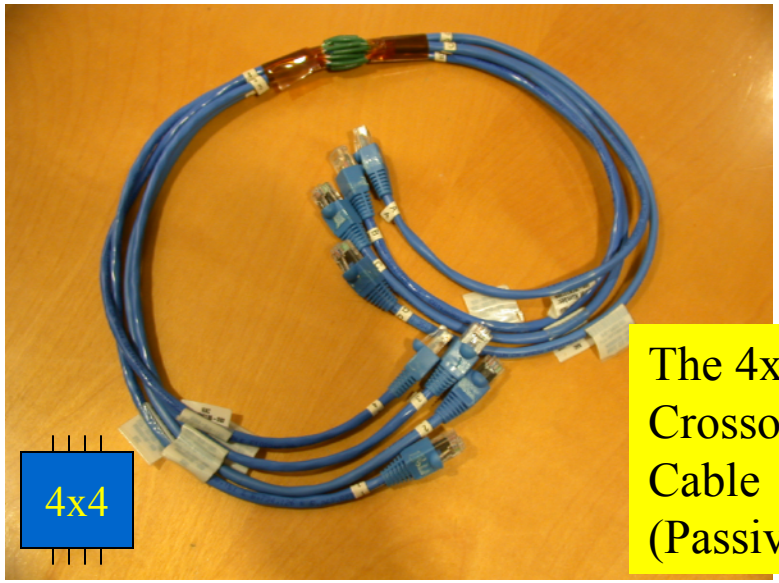
Partial Event Building (4x4)



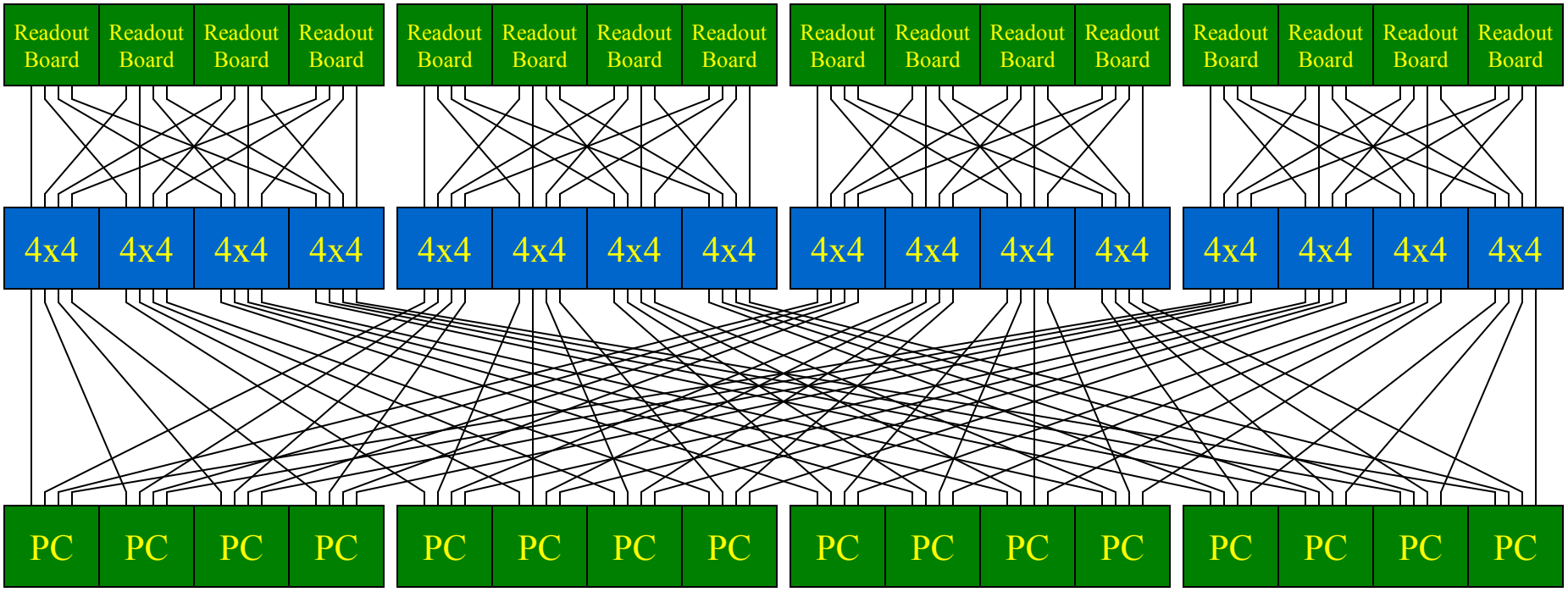
- 4 Data Receiver PCs handle 4 events from 4 Readout Boards.
- Each PC has information from 256 wires.
- With more wires seen, **safer** data **cut** can be done in software.
- For example, Stephen's hit parameterization scheme can be applied on tracks that are not overlapped with other tracks.
- Data volume is reduced **before sending into the DAQ switch**.
- With 16x16 partial event building, 1024 wires can be seen in each PC. See next page.

Partial Event Building (16x16)

- Each PC serves 16 Readout Boards, seeing 1024 wires.

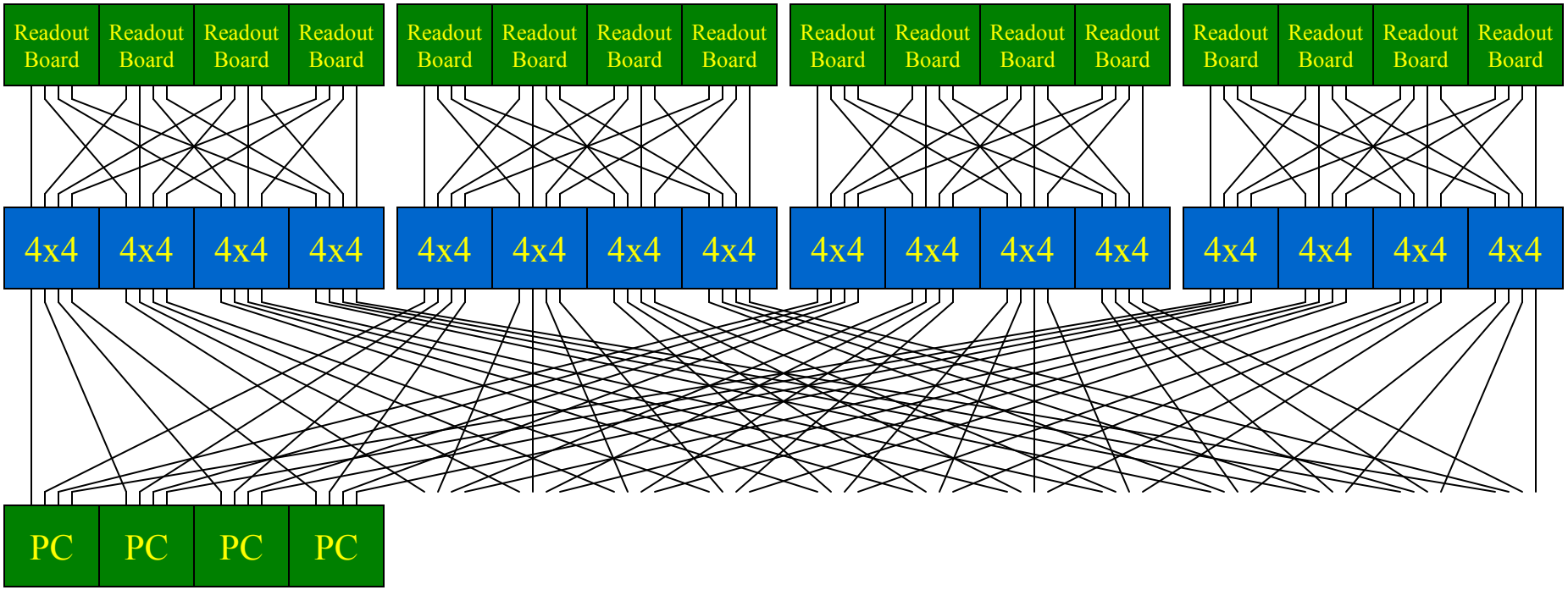


The 4x4 Crossover Cable (Passive)



Partial Event Building (16x4)

- In actual implementation, 1-16 PCs can be used. Each PC still serves all 16 Readout Boards, i.e., 1024 wires.
- In normal operation, if any data receiver PC fails, data can be routed to other PCs so that the whole system will still maintain operation.

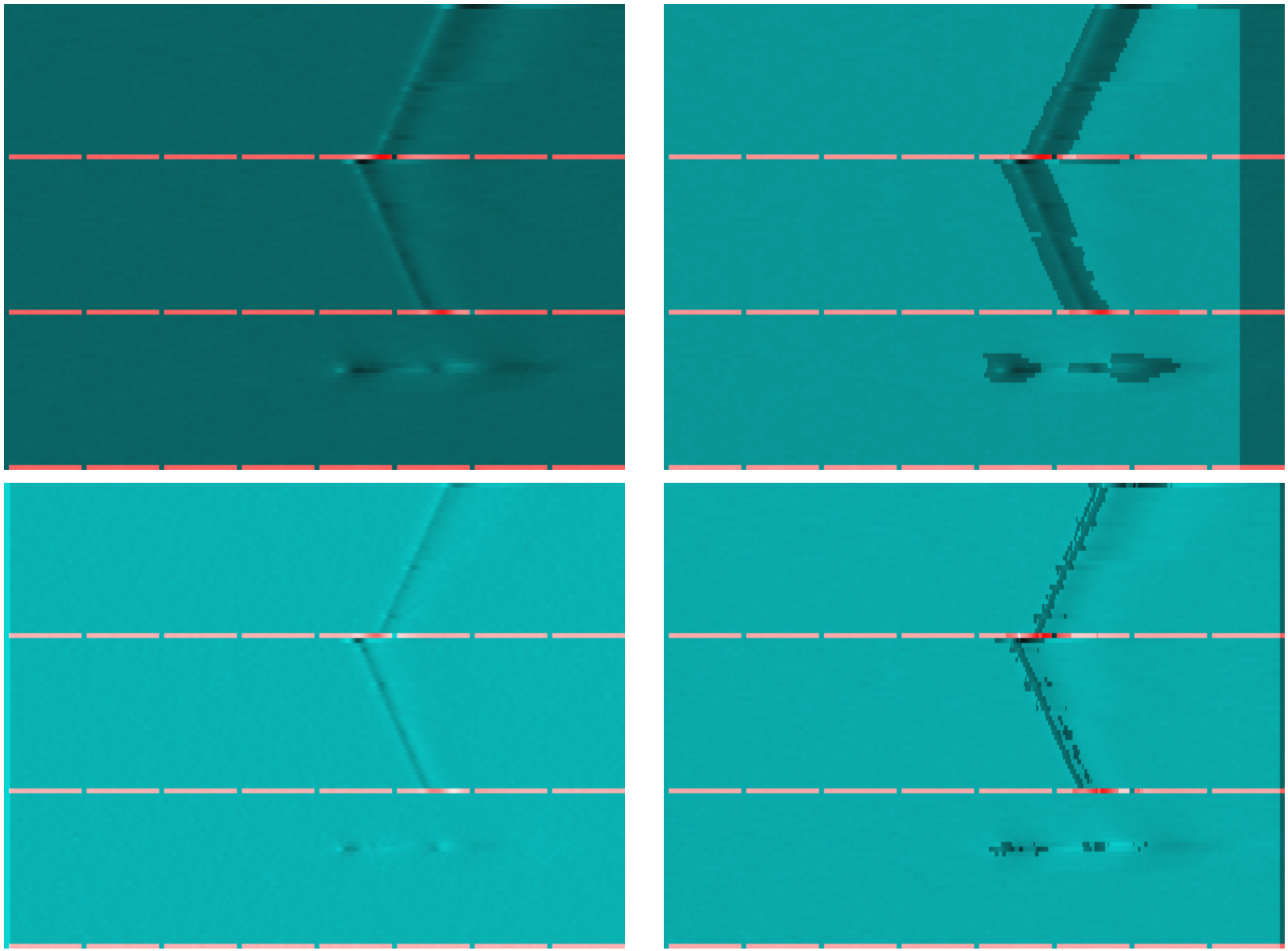


Summary

- DC operation, i.e., collecting all data, with good compression is not totally impossible.
- Again, do not give Chen a hard time. Save your questions for Wu after he comes back ☺

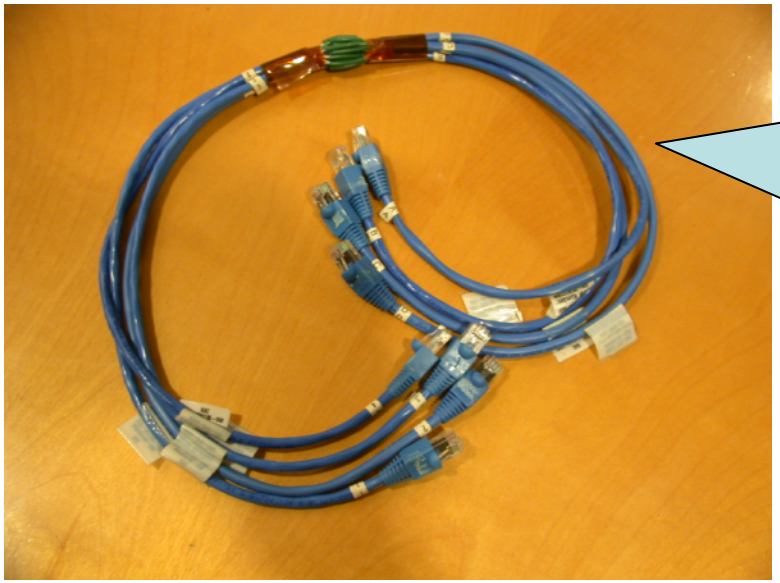
The End

Event Display: R089_E104

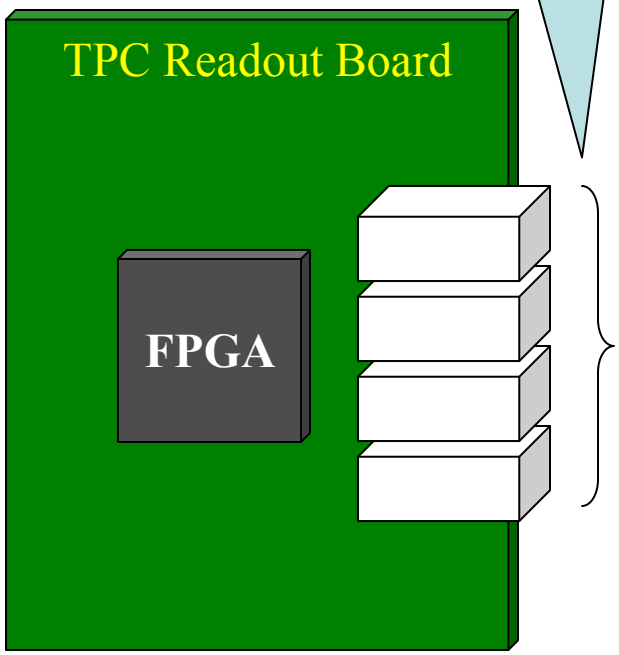


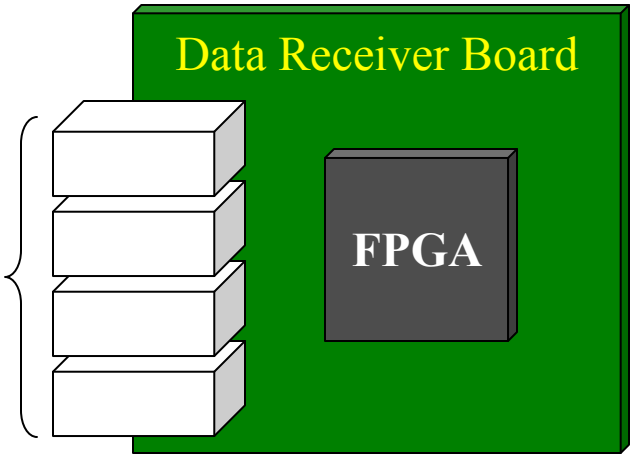
Partial Event Building (16x16)

The 4 RJ-45 connectors have 16 serial links, each sends data to one Data Receiver PC.



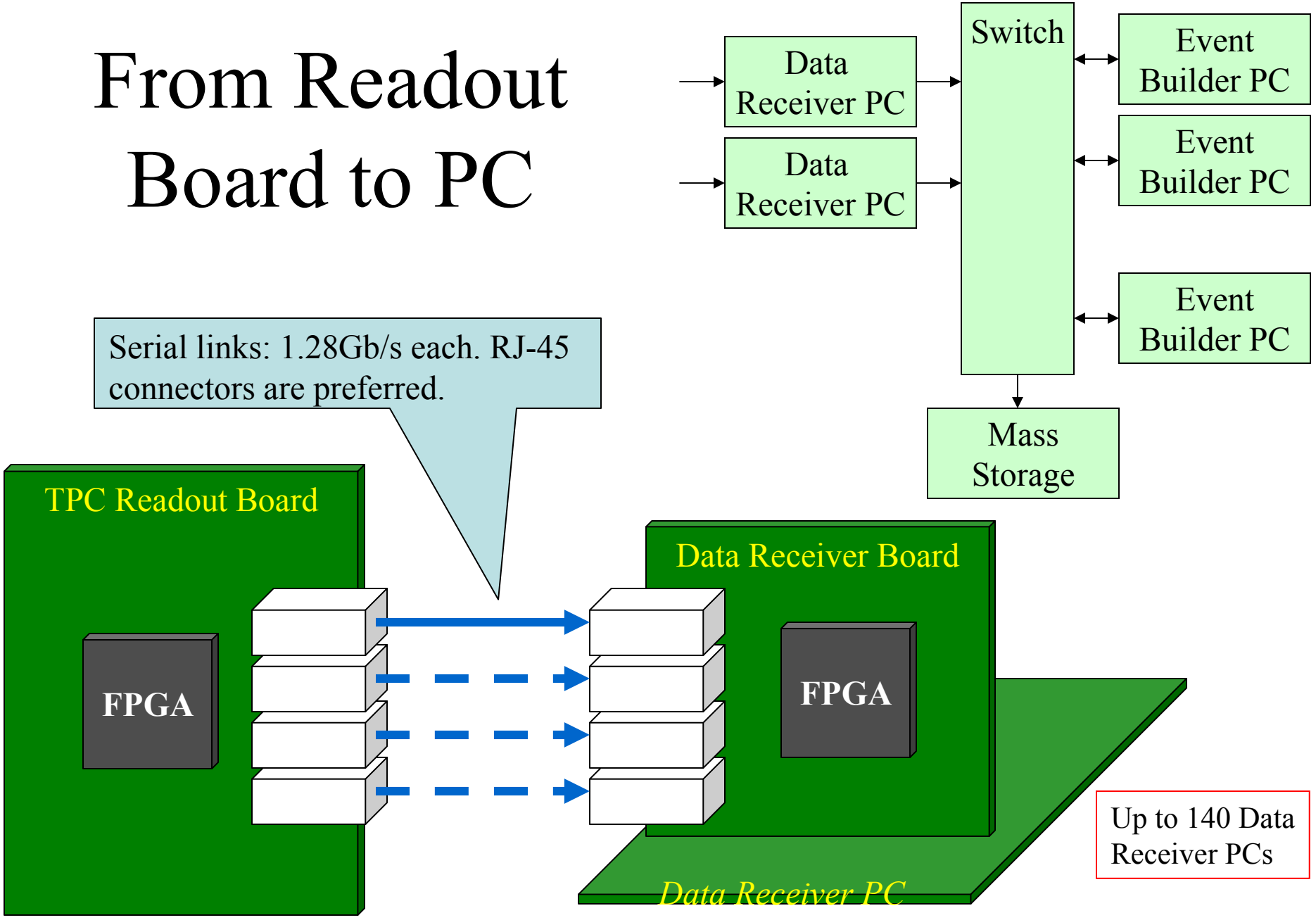
Use 4 sets of 4x4 crossover cables to interconnect 16 TPC Readout Boards and 16 Data Receiver PCs.



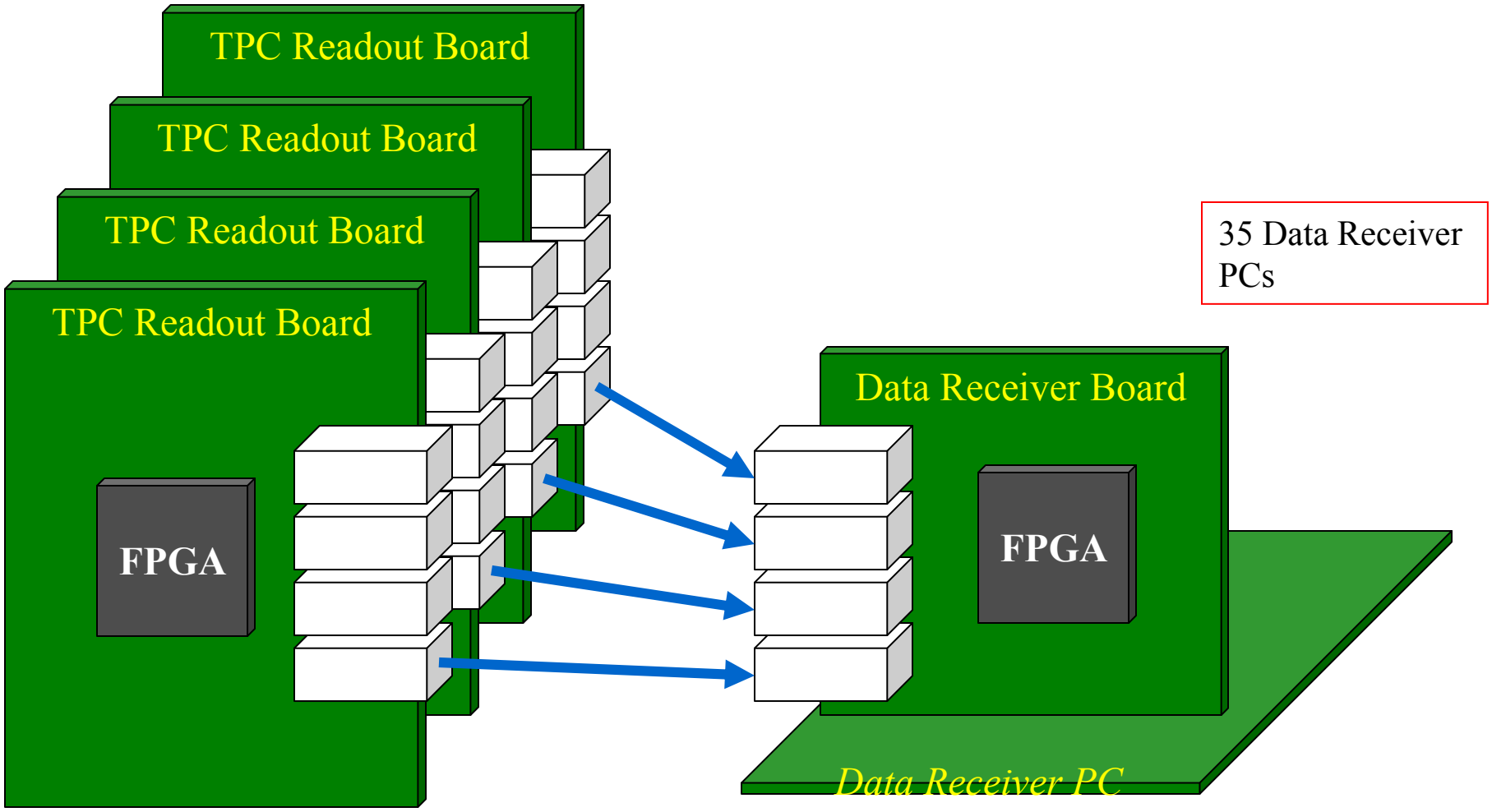


The 4 RJ-45 connectors have 16 serial links, each receives data from one TPC Readout Board.

From Readout Board to PC



Stage 1


TPC Readout Board
TPC Readout Board
TPC Readout Board
TPC Readout Board
FPGA
Data Receiver Board
FPGA
Data Receiver PC
35 Data Receiver PCs