

Micro-BooNE LArTPC FPGA Processing

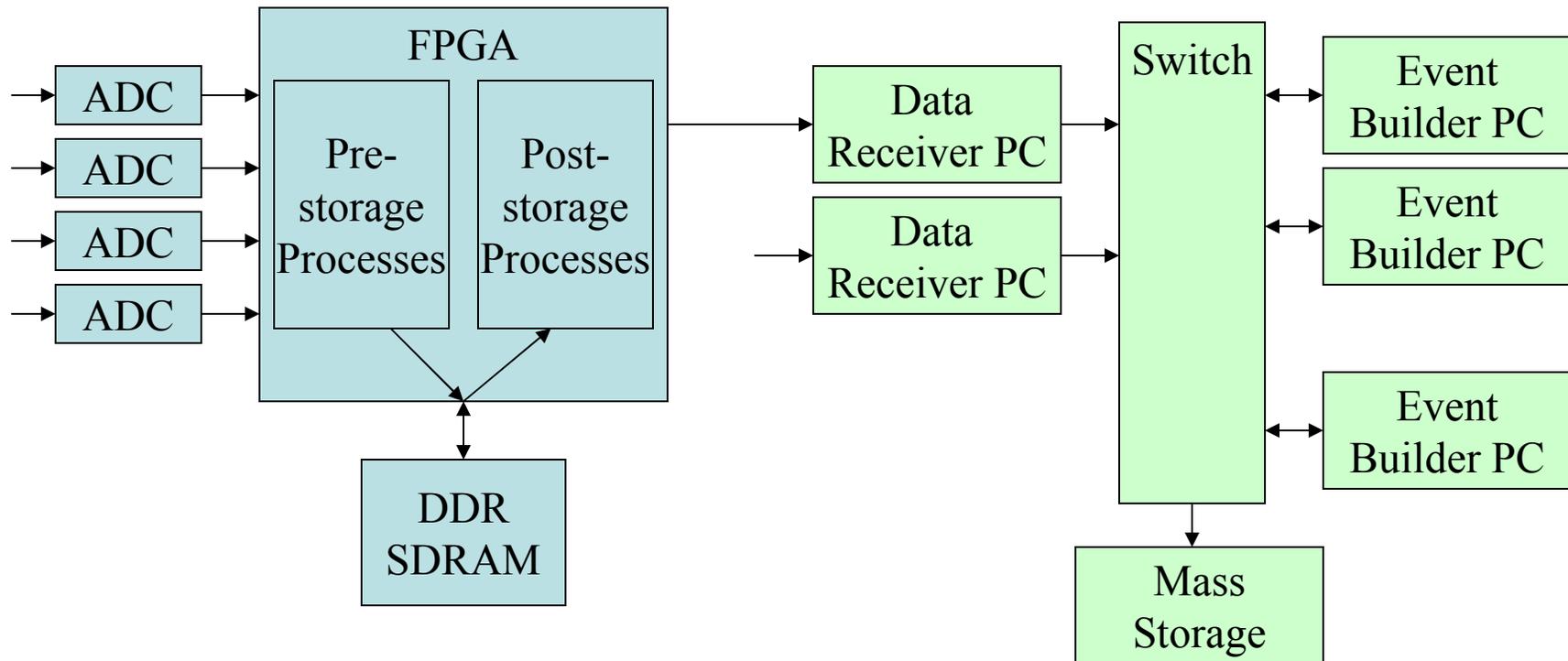
Wu, Jinyuan

Fermilab

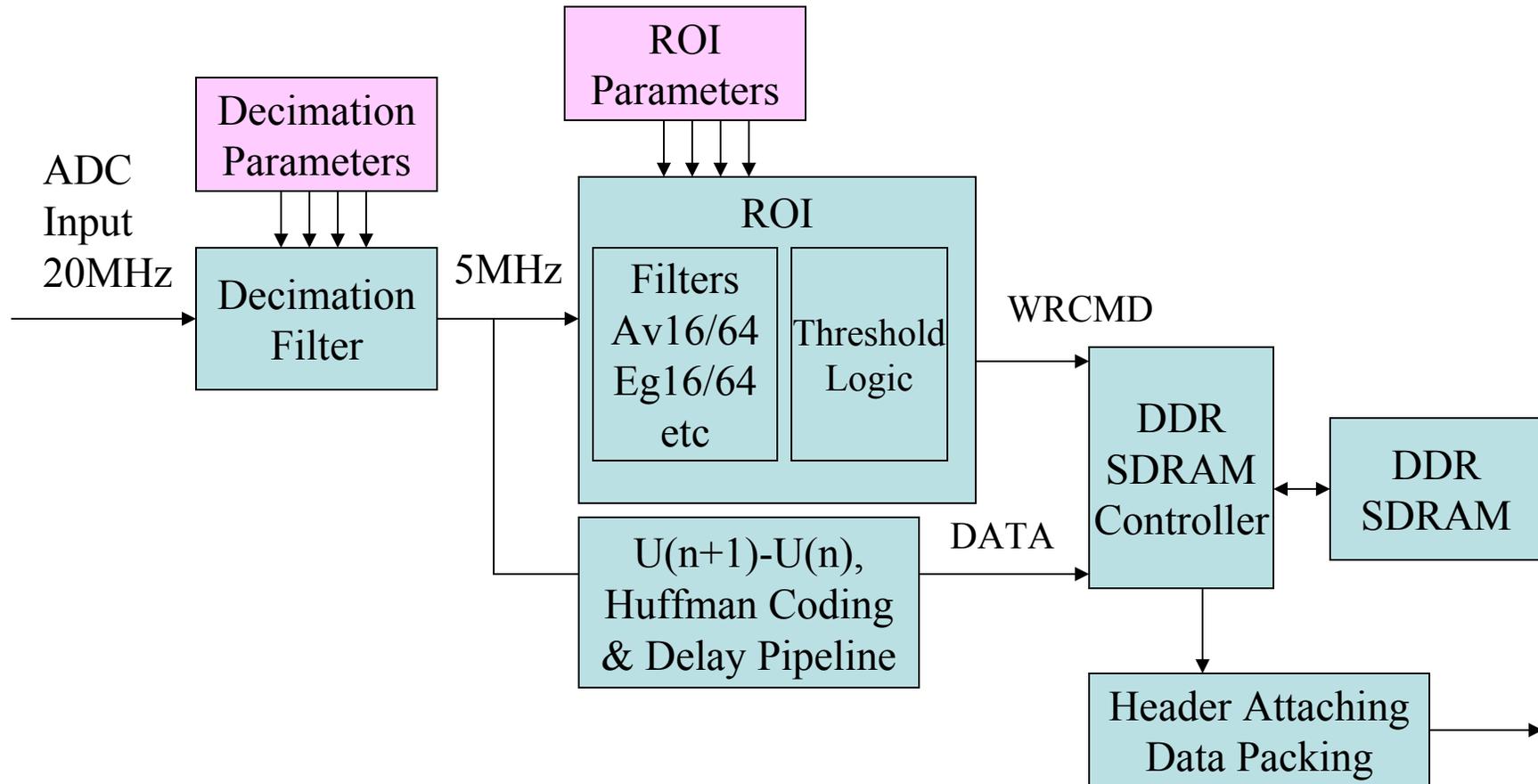
Nov. 2008

Introduction

- All processes in FPGA are **lossless** only.
- All data **deletions** can be deferred to PCs.
- FPGA may also calculate data selection **suggestions** for PCs to improve process speed in PCs.

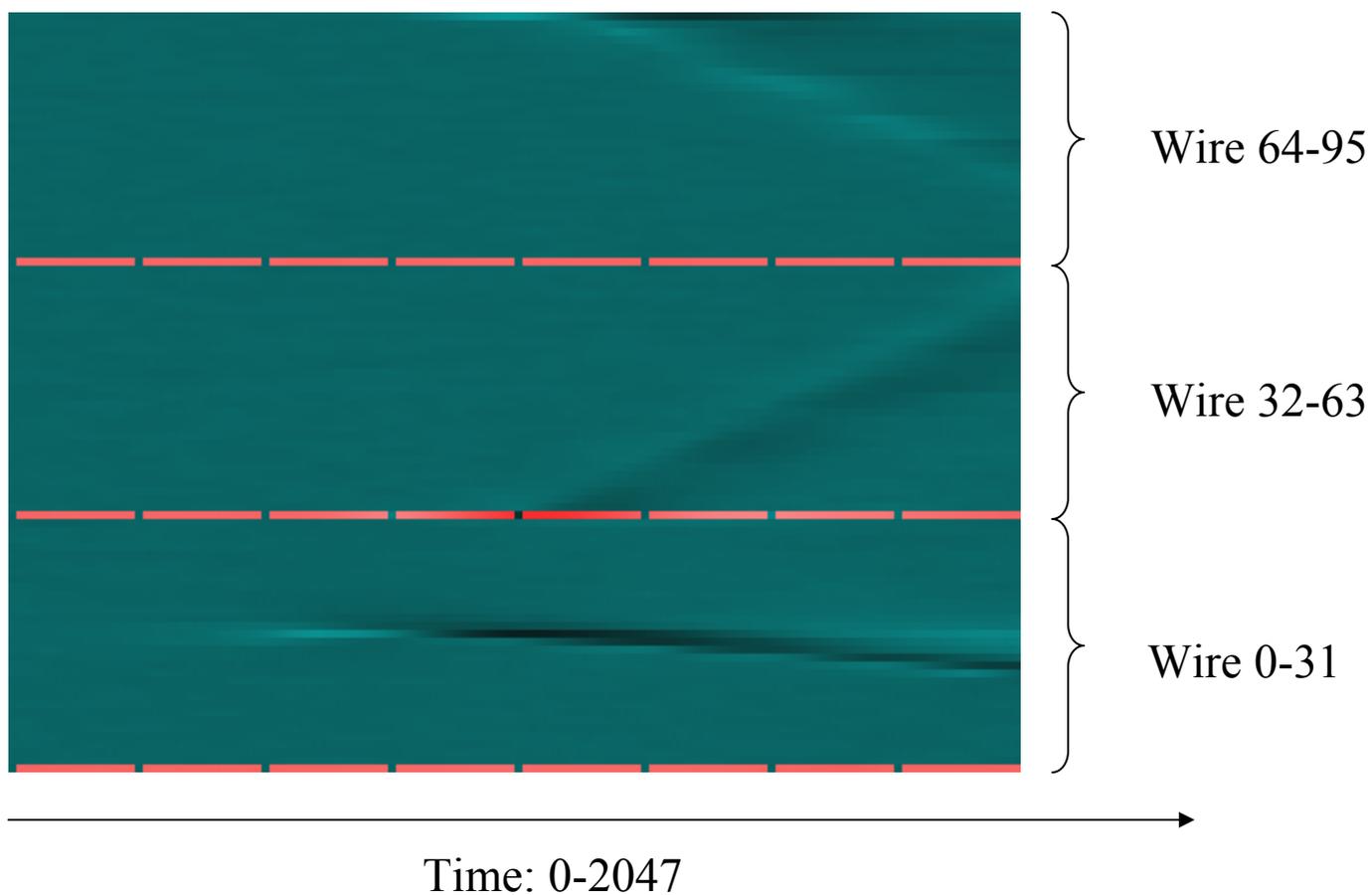


Details in FPGA

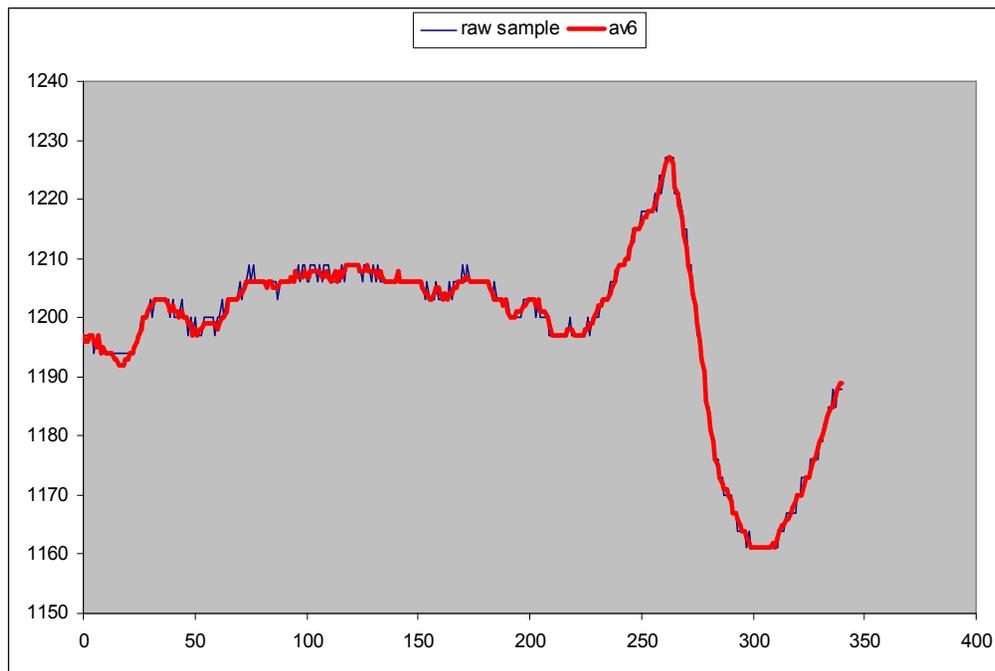


- The process time is $O(n)$, i.e., no large buffers are needed in FPGA.
- Processes parameters are programmable.

30MHz Event Display: R156_E101

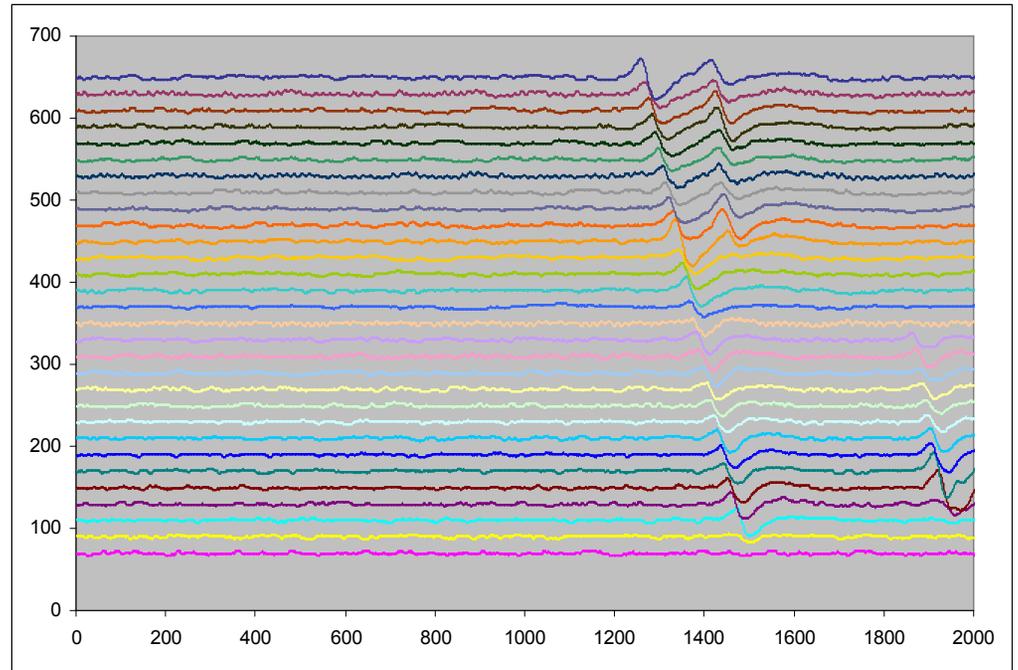
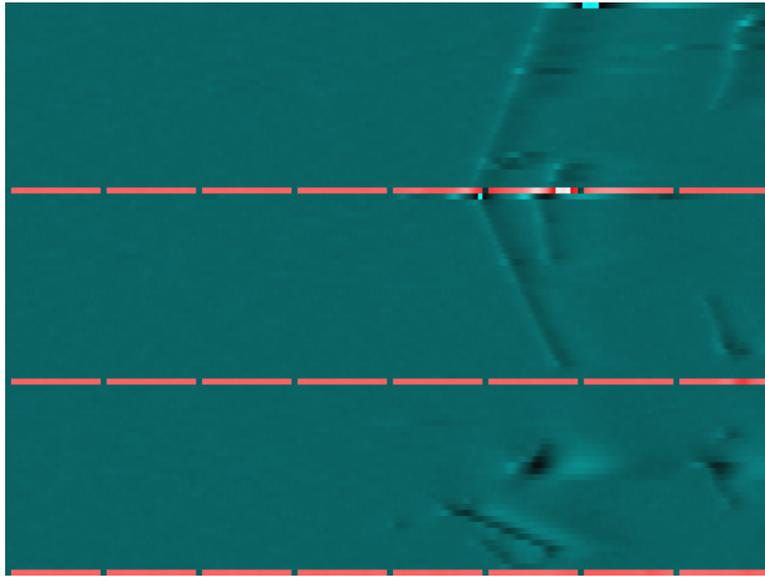


The 30MHz Data: $-30\text{MHz}/6$

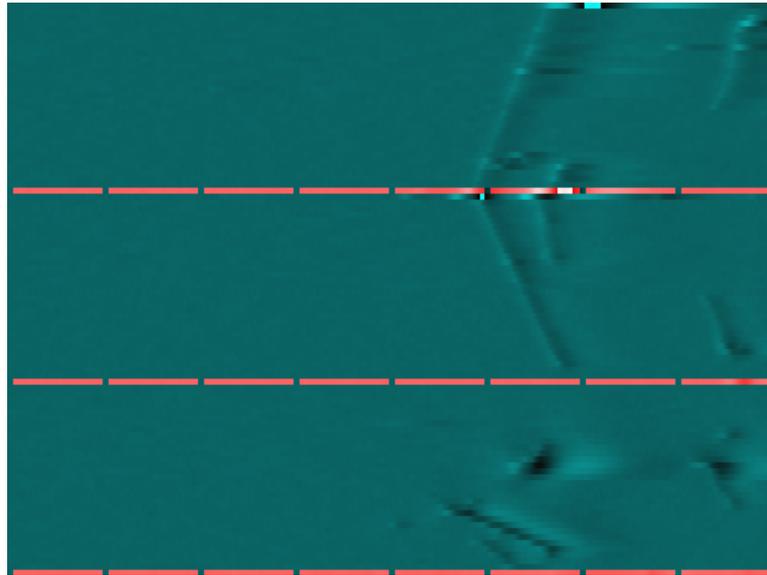


- Raw Sample: 1 out of 6.
- Av6: average of 6.
- Averaging reduces high frequency noise but not low frequency noise.
- The implementation cost is very low.
- The decimation filtering is considered a “standard” procedure. It provides additional safe guard for robust performance in case noise level becomes high.

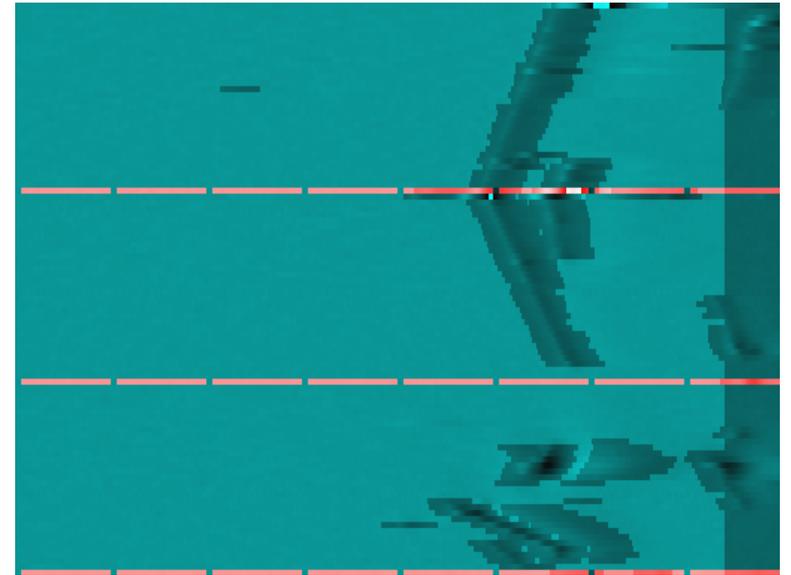
5 MHz Raw Data, R089_E175, W333-62



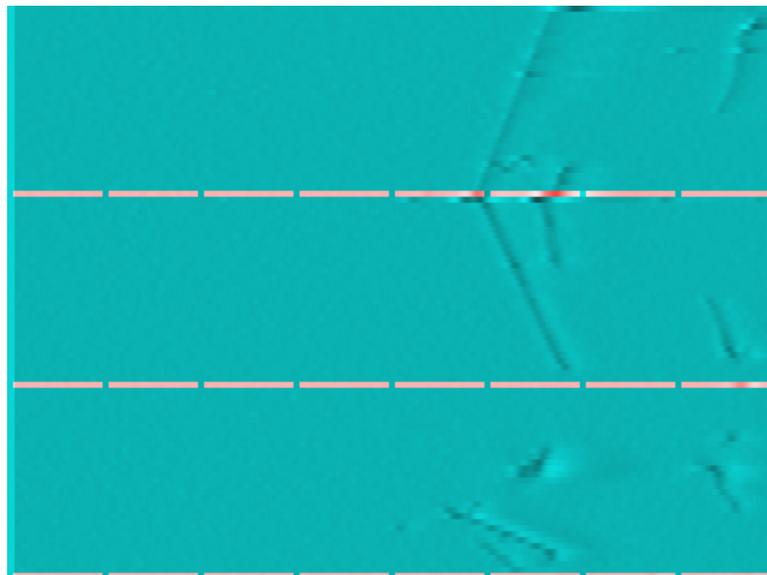
5MHz Event Display: R089_E175



Raw
Data



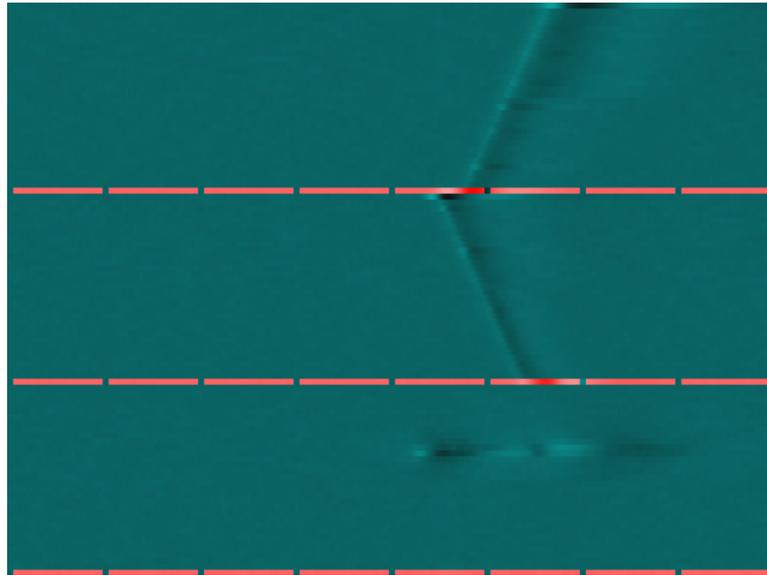
ROI, $|U(n+70)-U(n)| > 10$ in 100pt



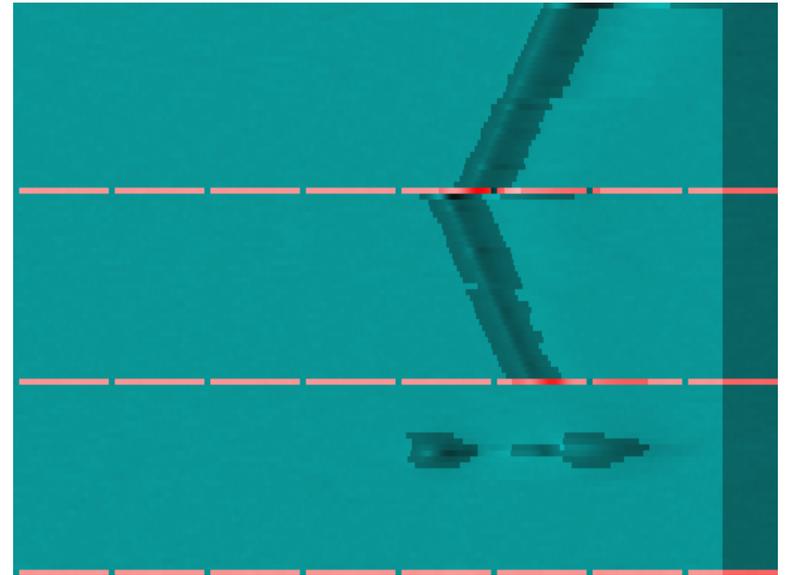
$U(n)-U(n-20)$

See also Doug Jensen's talk

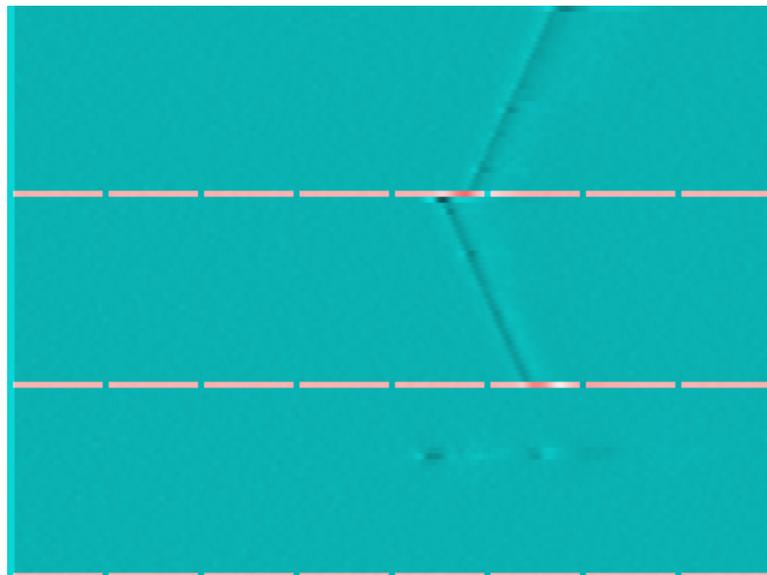
5MHz Event Display: R089_E104



Raw
Data

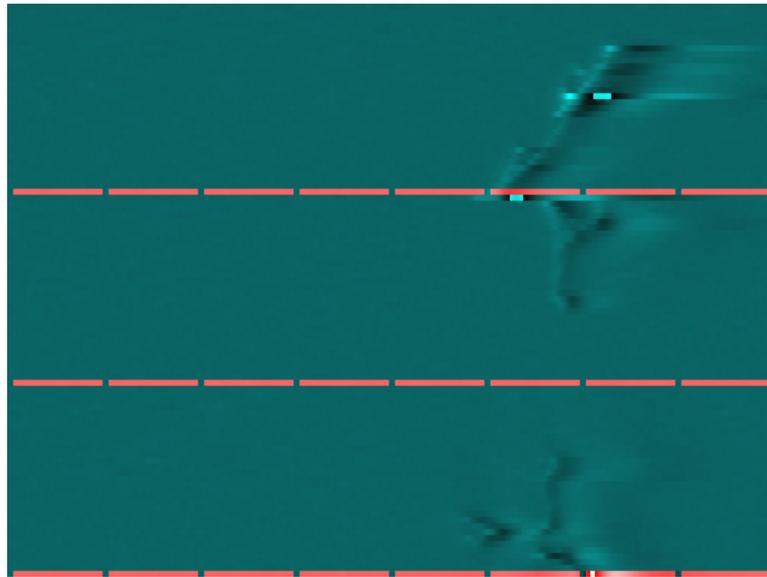


ROI, $|U(n+70)-U(n)| > 10$ in 100pt

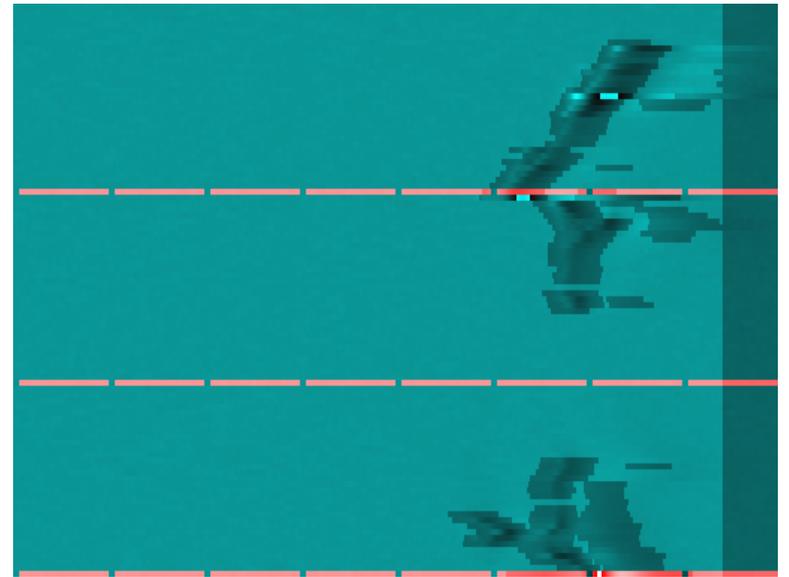


$U(n)-U(n-20)$

5MHz Event Display: R097_E115



Raw
Data

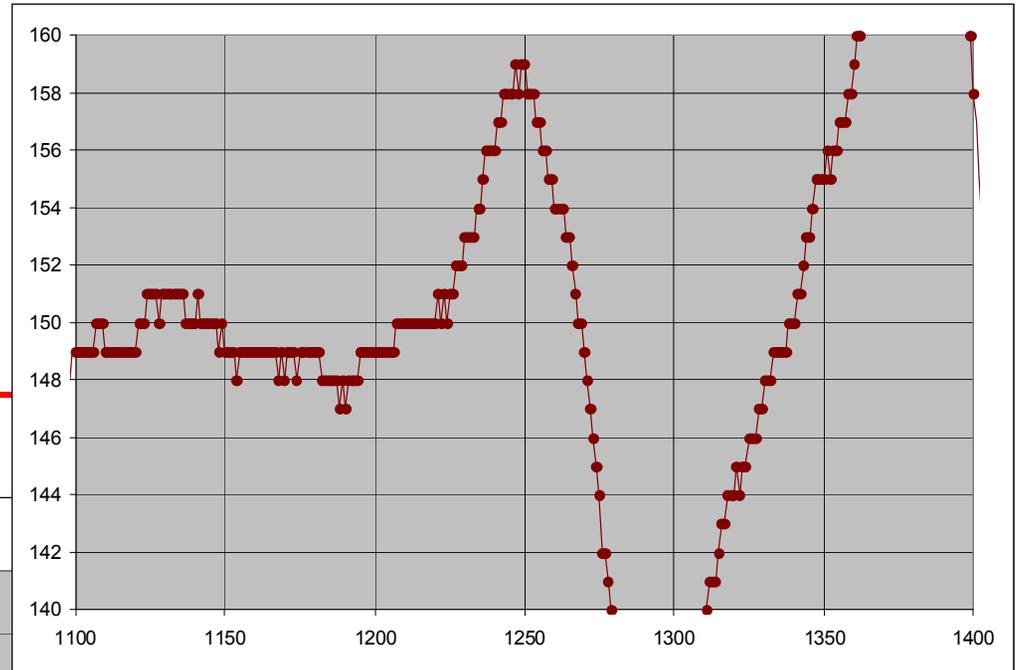
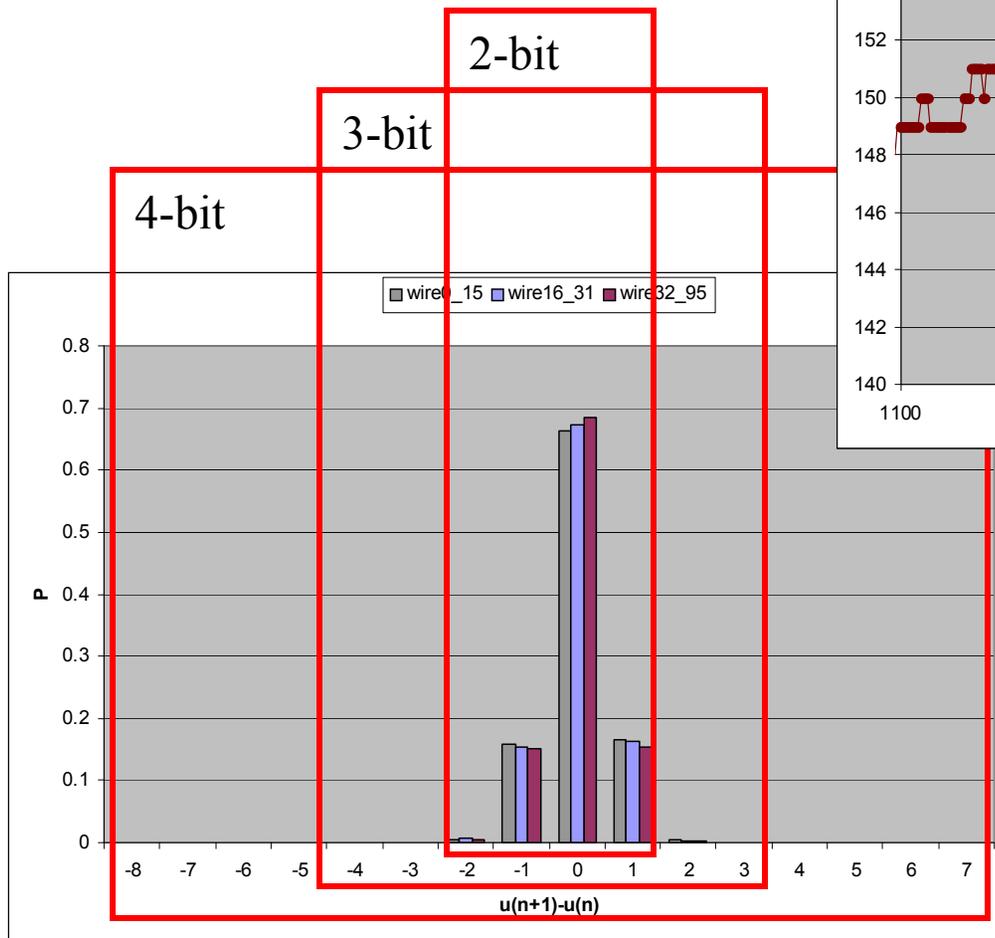


ROI, $|U(n+70)-U(n)| > 10$ in 100pt



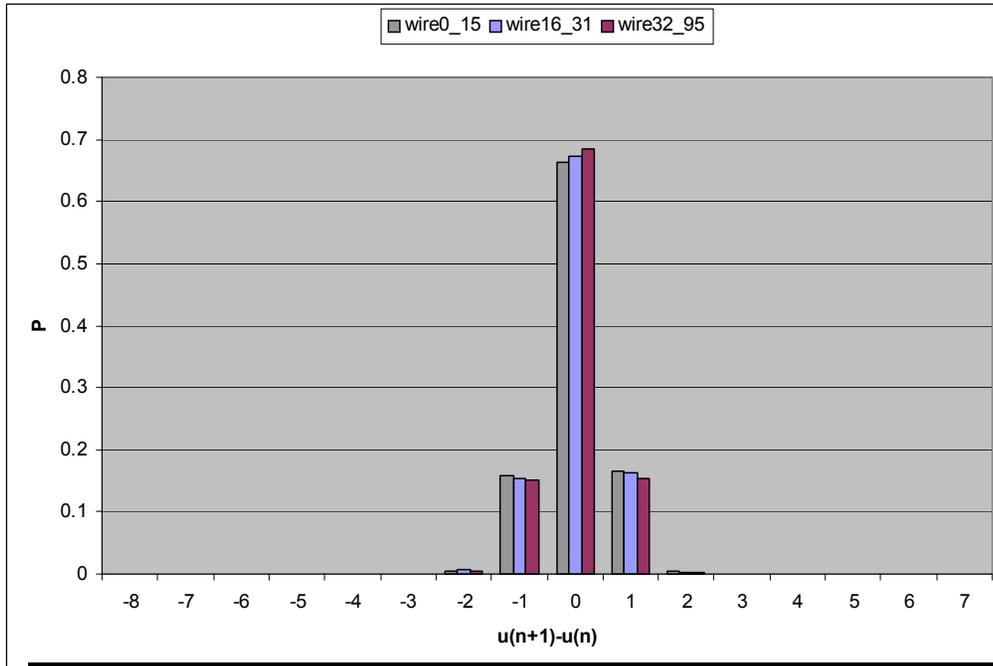
$U(n)-U(n-20)$

Slow Variation of Raw Data



- More than 99% points can be represented with 2 bits.
- All points can be represented with 3 or 4 bits.

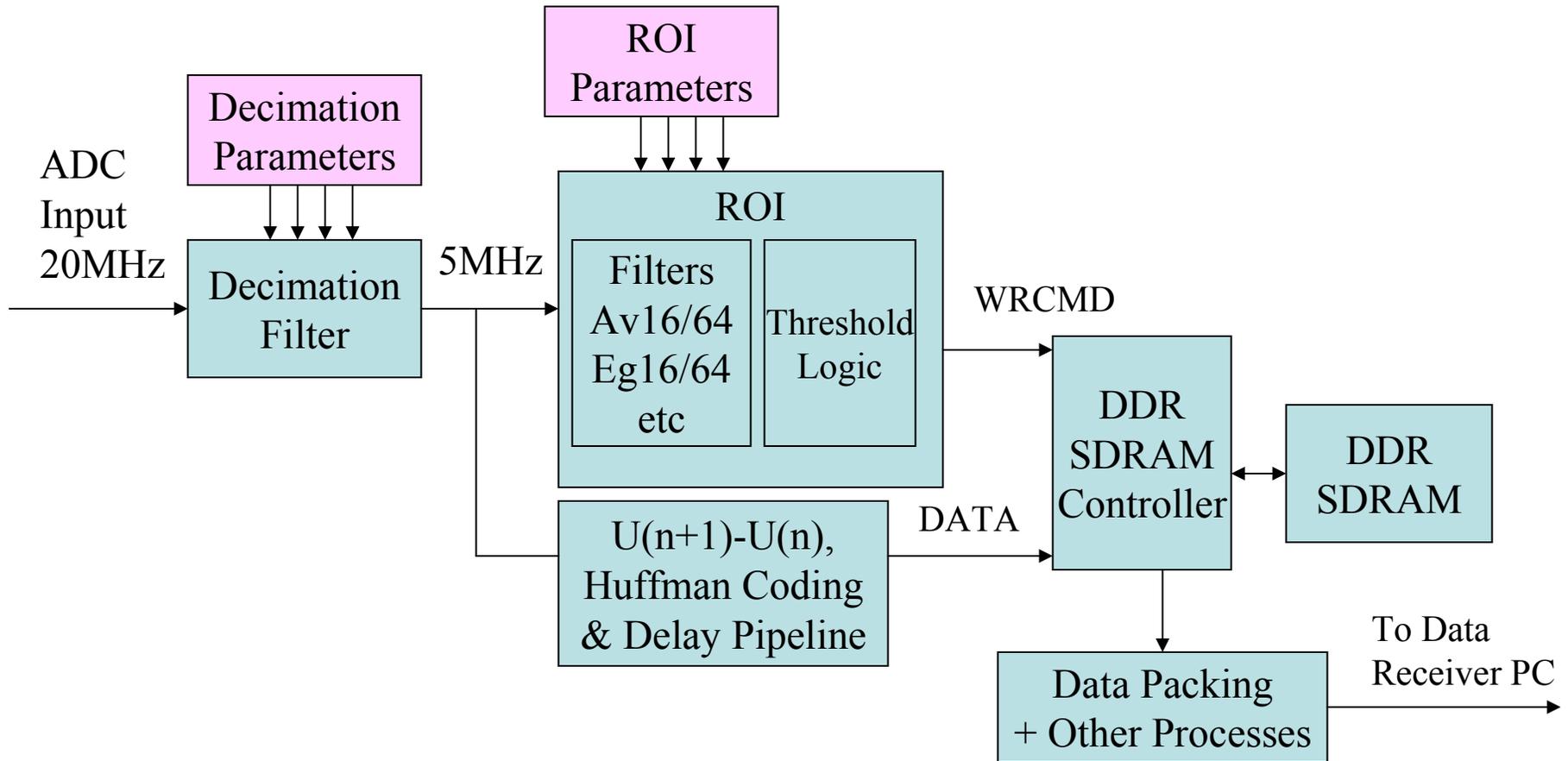
Huffman Coding



- Shorter codes (1-7 bits) are assigned to high P values from -3 to +3.
- Any values outside ± 3 use 16 bits.
- In this example, coding rate is **1.53 bits/sample**.
- In other examples coding rate is also ~ 1.5 bits/sample.

$U(n+1)-U(n)$	Count	Probability (P)	Code	No. of bits (N)	$P*N$
-4 and others	11	0.000179124	Full 16 bits word	16	0.002866
-3	45	0.00073278	111110	6	0.004396
-2	358	0.005829669	1110	4	0.023318
-1	9681	0.157645335	10	2	0.315290
0	40867	0.665477935	0	1	0.665477
+1	10145	0.165201107	110	3	0.495603
+2	298	0.00485263	11110	5	0.024263
+3	5	8.142E-05	1111110	7	0.000569
total		1.00			1.53

Details in FPGA



- The process time is $O(n)$, i.e., no large buffers are needed in FPGA.
- Processes parameters are programmable.

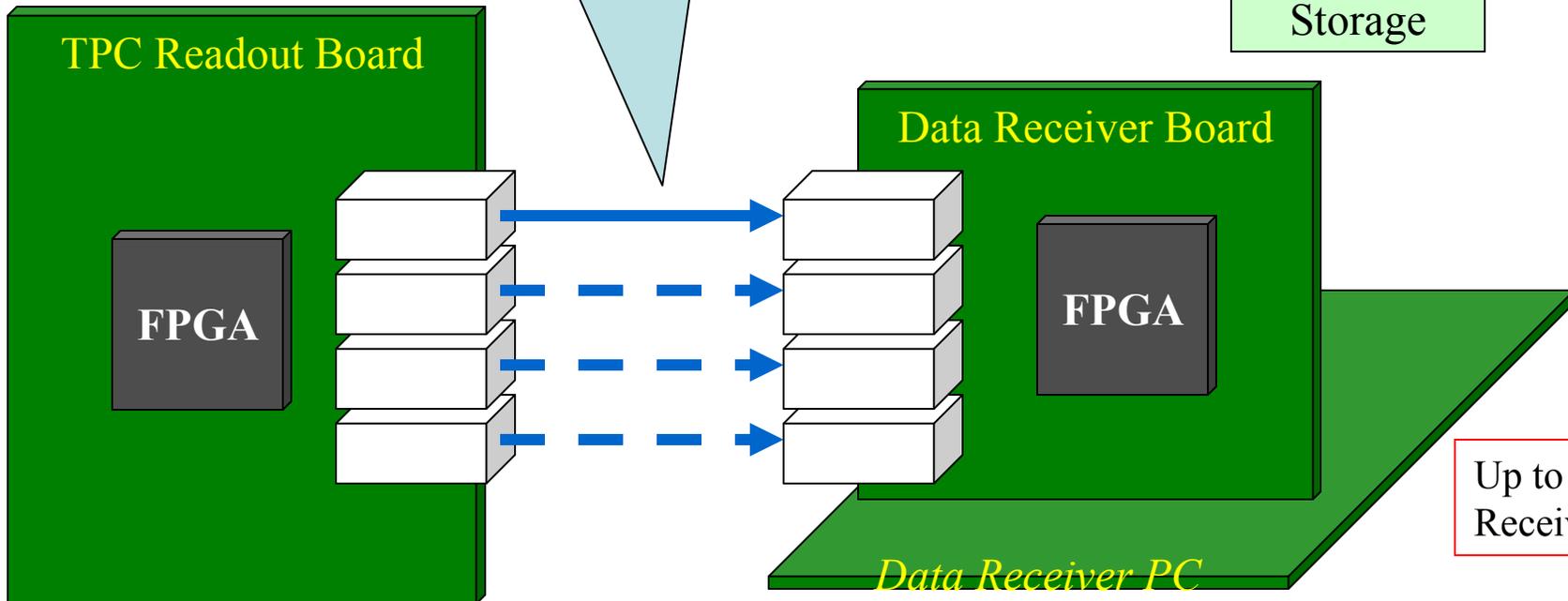
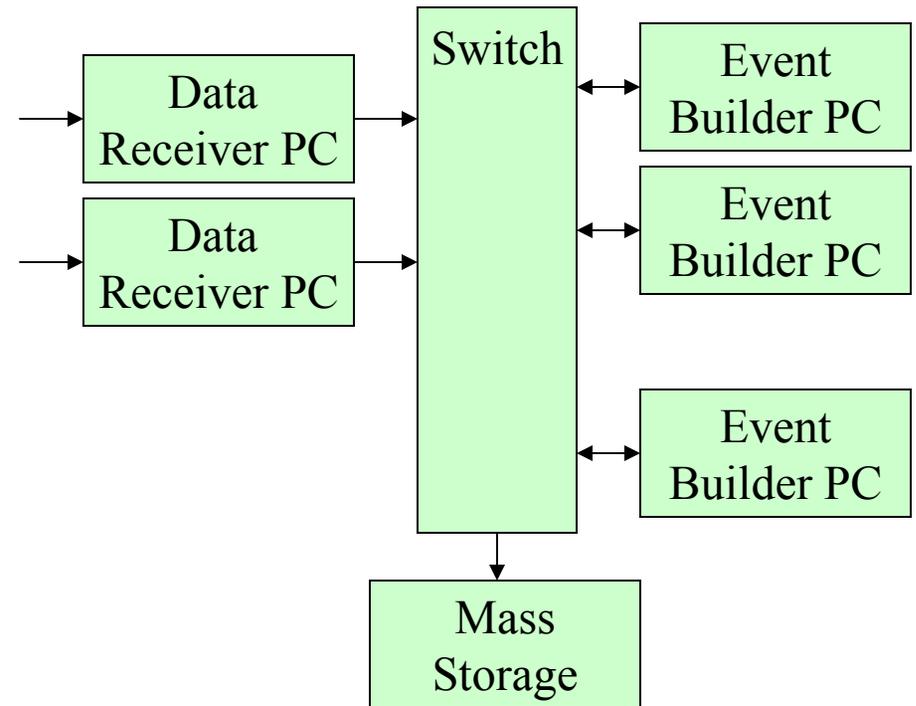
Data Rate for Storage in TPC Readout Board

Storage Mode & Rate	Transfers with 64-bit SDRAM for 64 channels	Storage Capacity 256 MB	Data Rate to PC (/Board)
Chronicle 5 MHz	80 M Trans./s	0.4 sec	5.12Gb/s
Huffman Coding 4bits/sample, 5 MHz	Peak: same as above Av: 20 M Trans./s	1.6 sec	1.28Gb/s
ROI: 6kHz x 2K wires x 100 points (From Stephen P.)	Peak: same as above Average: 6k x (2K/12K) x 100 x 64 = 6.4 M Points/s = 1.6 M Trans./s	20 sec.	102Mb/s

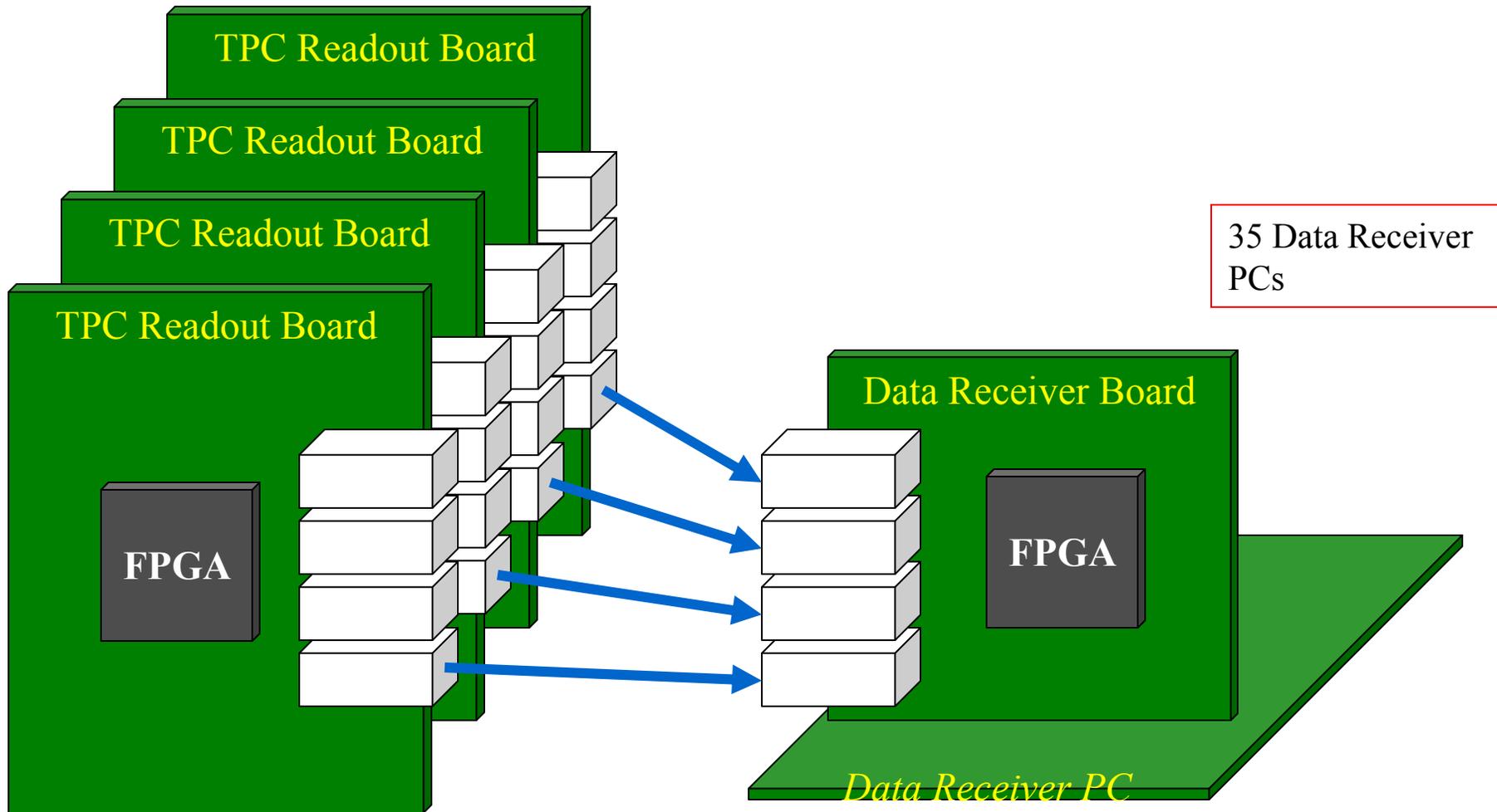
- One RJ-45 connector: 4pairs x 320Mb/s/pair = 1.28Gb/s.
- Four RJ-45 connectors: 5.12Gb/s.
- The data rate for the links to operate is intended to be as low as possible.

From Readout Board to PC

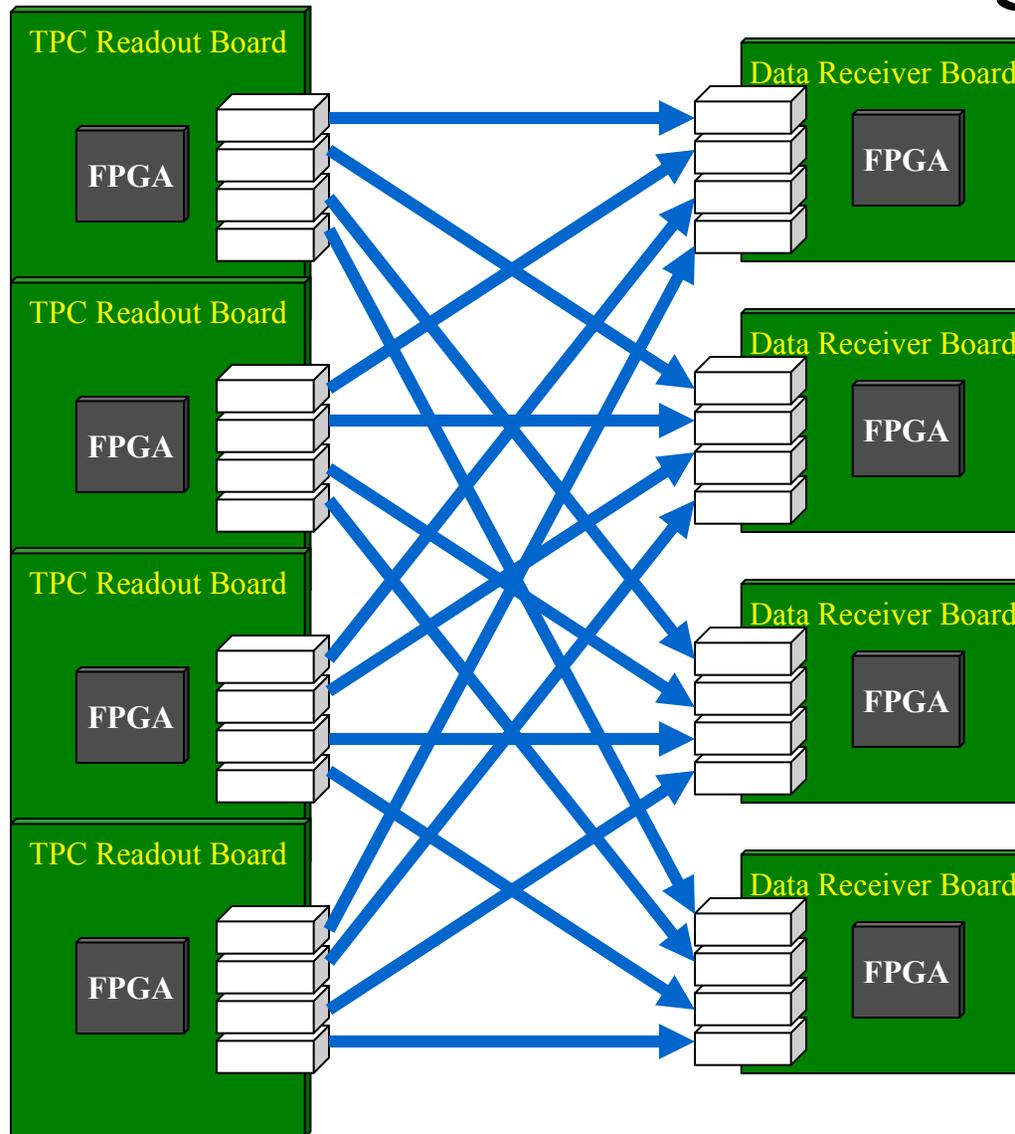
Serial links: 1.28Gb/s each.
RJ-45 connectors are sufficient. Optical links are OK if they are affordable.



The Early Commissioning Stage

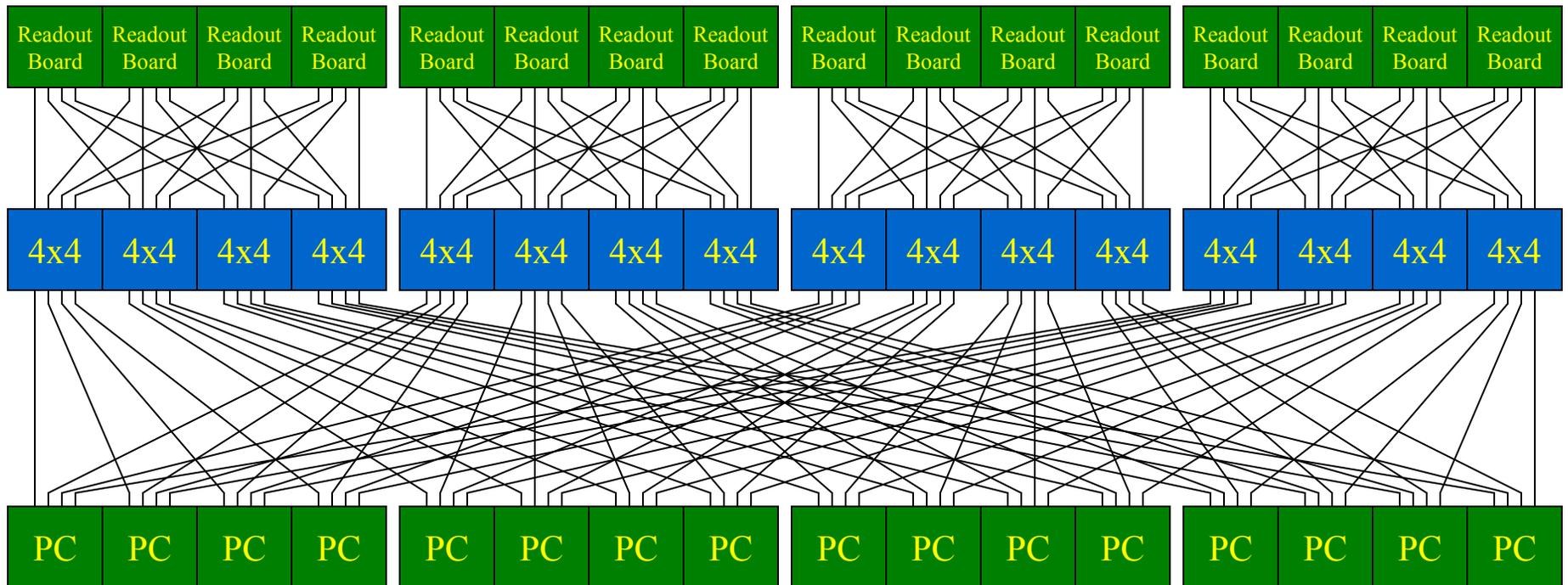
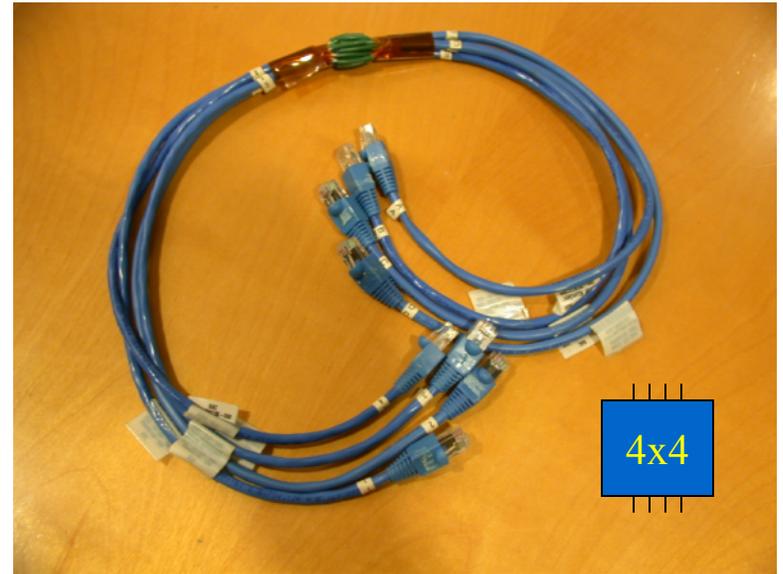


Partial Event Building (4x4)

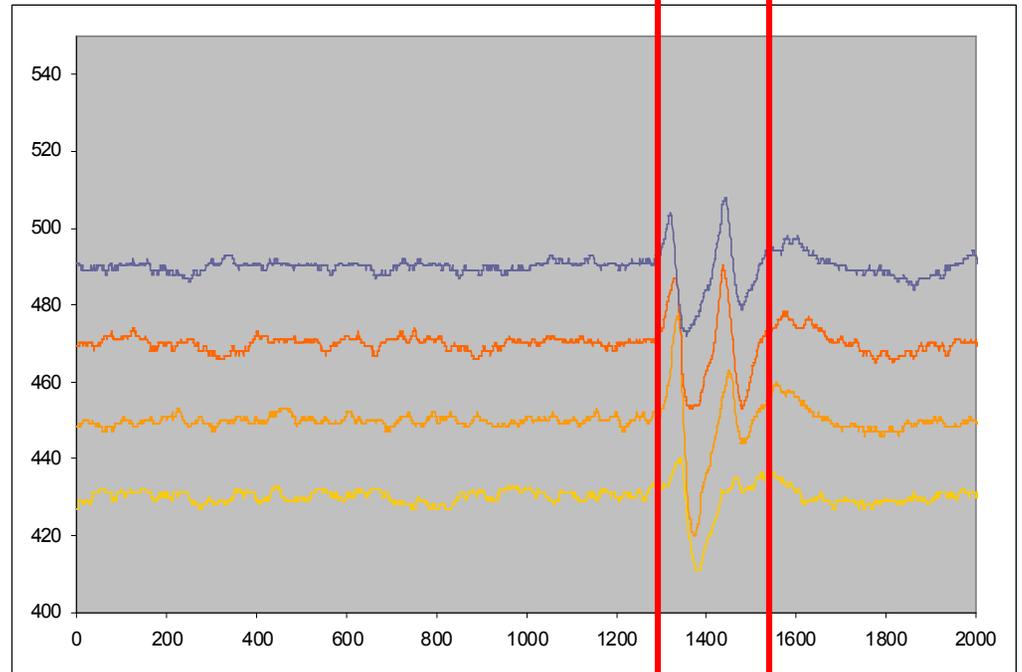
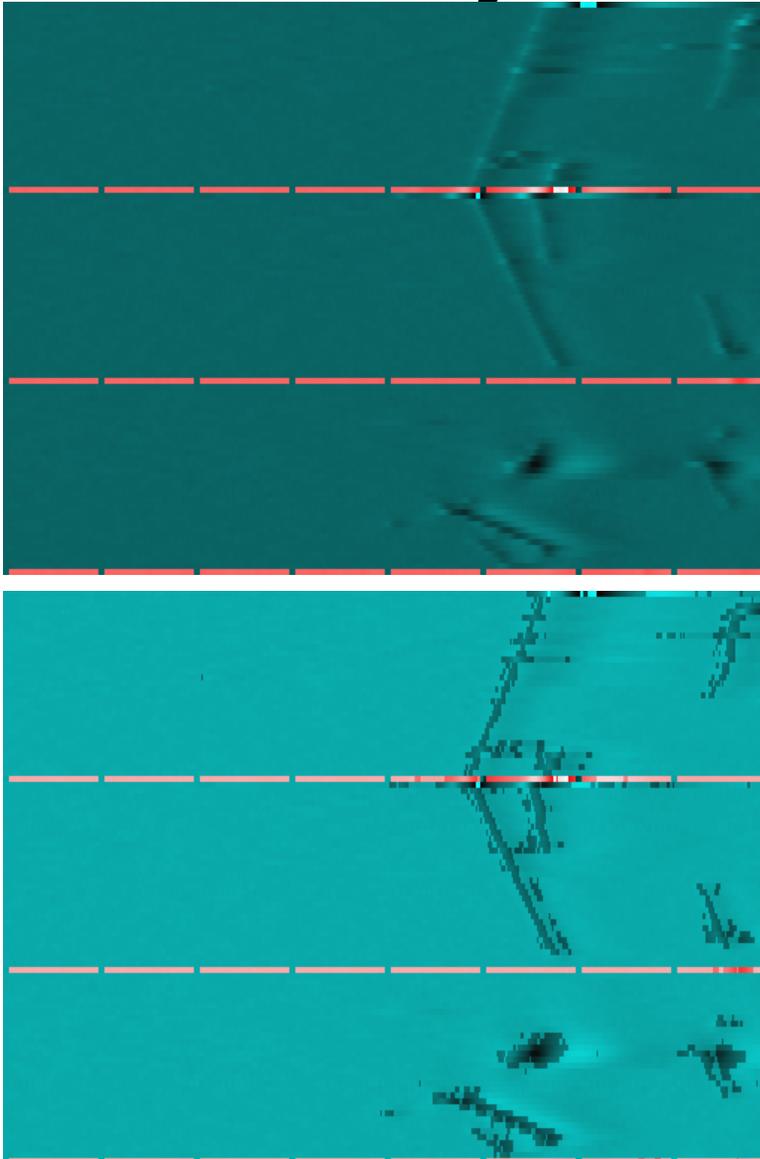


4 Data Receiver
PCs handle 4 events from
4 Readout Boards.

Partial Event Building (16x16)

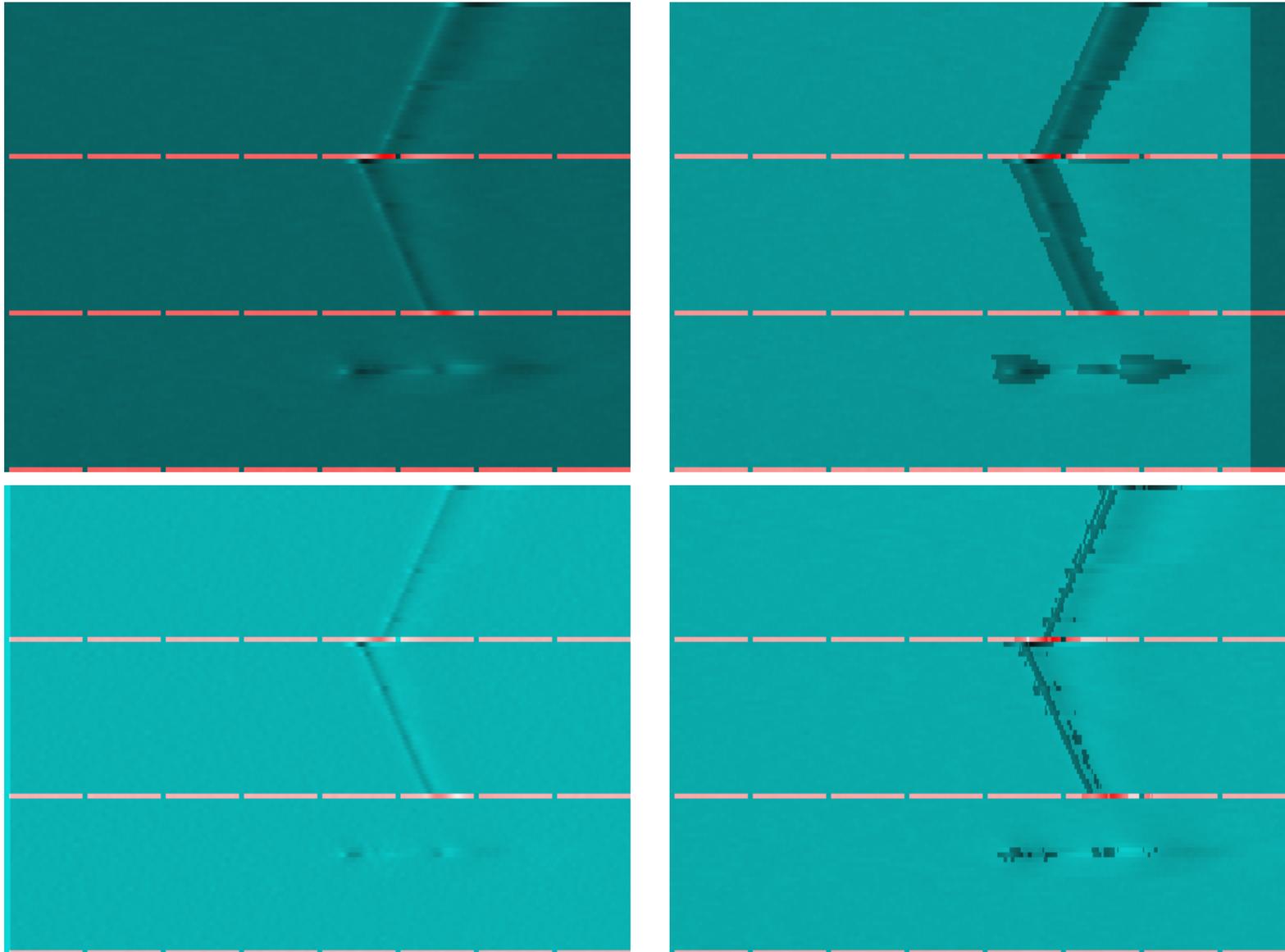


Dynamic Decimation



- Only small time intervals must be sampled at 5MHz.
- Most time intervals can be sampled with lower frequency, e.g., (5/16)MHz without losing useful information.
- The excessive data can be **tagged** in FPGA and **deleted** in PC.

Event Display: R089_E104



Nov. 2008

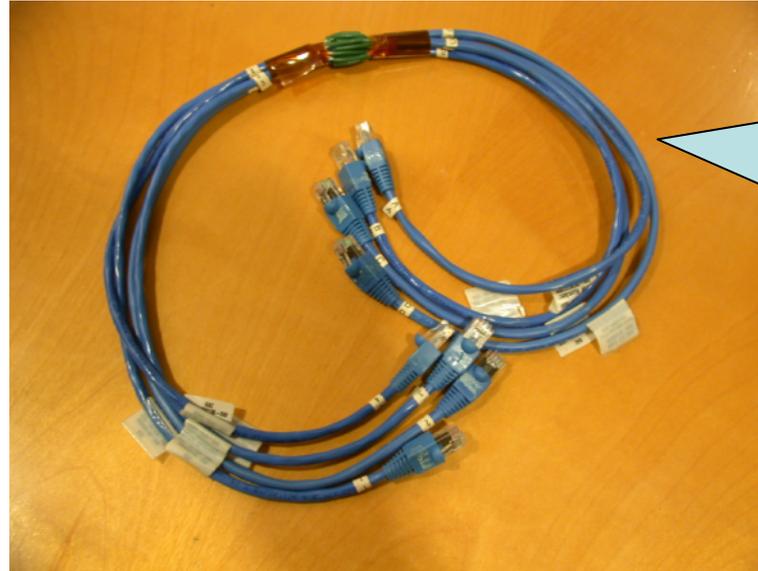
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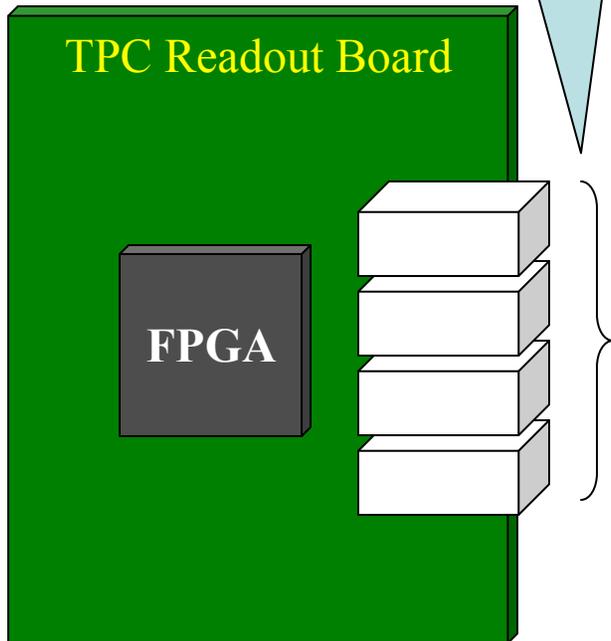
The End

Partial Event Building (16x16)

The 4 RJ-45 connectors have 16 serial links, each sends data to one Data Receiver PC.



Use 4 sets of 4x4 crossover cables to interconnect 16 TPC Readout Boards and 16 Data Receiver PCs.



The 4 RJ-45 connectors have 16 serial links, each receives data from one TPC Readout Board.

